# Anticipated Acquisition by Synopsys, Inc. of ANSYS, Inc.

## Decision on relevant merger situation and substantial lessening of competition

**ME 7101/24**

The Competition and Markets Authority's decision on relevant merger situation and substantial lessening of competition under section 33(1) of the Enterprise Act 2002 given on 20 December 2024. Full text of the decision published on 3 February 2025.

The Competition and Markets Authority (**CMA**) has excluded from this published version of the decision information which the CMA considers should be excluded having regard to the three considerations set out in section 244 of the Enterprise Act 2002 (specified information: considerations relevant to disclosure). The omissions are indicated by [✂]. Some numbers have been replaced by a range, which are shown in square brackets.

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# SUMMARY

## OVERVIEW OF THE CMA'S DECISION

1. The Competition and Markets Authority (**CMA**) has found that the acquisition by Synopsys, Inc. (**Synopsys**) of ANSYS, Inc. (**Ansys**), gives rise to a realistic prospect of a substantial lessening of competition (**SLC**) as a result of horizontal unilateral effects in the global supply of (i) register-transfer-level (**RTL**) power consumption analysis for digital chips; (ii) optics software; and (iii) photonics software.

2. Synopsys has agreed to acquire Ansys pursuant to an agreement dated 15 January 2024. The CMA refers to this acquisition as the **Merger**. Synopsys and Ansys are together referred to as the **Parties** and, for statements relating to the future, the **Merged Entity**.

3. As the CMA has found that the Merger gives rise to a realistic prospect of a substantial lessening of competition (an **SLC**) in the UK, the Parties have until 31 December 2024 to offer undertakings in lieu of a reference (**UILs**) to the CMA that will remedy the competition concerns identified. If no such undertaking is offered, then the CMA will refer the Merger for an in-depth phase 2 investigation pursuant to sections 33(1) and 34ZA(2) of the Enterprise Act 2002 (the **Act**).

### Who are the businesses and what products/services do they provide?

4. Synopsys, headquartered in the United States and listed on the Nasdaq Global Select Market, is a global software supplier. One of its main business segments is the supply of electronic design automation (**EDA**) software, which allows customers to design semiconductors (integrated circuits, or **chips**). EDA software helps chip design customers and 'system' customers (such as aerospace and mobile phone manufacturers that use chips in their products) to plan, design and verify chips before they are sent for manufacturing. Synopsys also supplies optics and photonics software, which is used to design and simulate light-related products like camera lenses and lasers for customers in a wide range of industries.

5. Ansys, also headquartered in the United States and listed on the Nasdaq Global Select Market, is a global EDA software and multiphysics simulation and analysis (**S&A**) software supplier. S&A software is used to simulate and analyse the behaviour of products, systems or processes digitally and is used across a wide range of industries including semiconductors, aerospace and defence and automotive. Like Synopsys, Ansys' EDA software products are also used by customers in the chip design process. Ansys' S&A software (which includes optics and photonics software) is also used by customers in a wide range of other industries.

## Why did the CMA review this merger?

6. The CMA's primary duty is to seek to promote competition for the benefit of consumers. It has a duty to investigate mergers that could raise competition concerns in the UK, provided it has jurisdiction to do so. In this case, the CMA has concluded that the CMA has jurisdiction to review this Merger because a relevant merger situation has been created: each of Synopsys and Ansys is an enterprise that will cease to be distinct as a result of the Merger and the share of supply test is met.

7. Synopsys announced on 16 January 2024 that it had agreed to acquire Ansys for a purchase price of approximately $35 billion. The Merger is undergoing merger control investigations by other competition authorities in multiple jurisdictions including but not limited to the EU, United States, Japan, and South Korea.

## What evidence has the CMA looked at?

8. In assessing this Merger, the CMA considered a wide range of evidence in the round.

9. The CMA received several submissions and responses to information requests from the Parties. The CMA gathered information about the Parties' current and pipeline products to better understand the extent to which they currently compete or may compete in future. The CMA requested and reviewed a significant number of the Parties' internal documents on their current and future strategy to understand how they run their businesses and how they view their rivals, including in the ordinary course of business. These internal documents were also helpful in understanding the Parties' plans for the future, including the rationale for the Merger.

10. The CMA spoke to and gathered evidence from other market participants, including competitors and a large range of customers of the Parties' products. This evidence included both written and oral submissions, which the CMA reviewed to better understand the competitive landscape and to get market participants' views on the impact of the Merger.

## What did the evidence tell the CMA about the effects on competition of the Merger?

11. The CMA carefully examined the overlaps and relationships between Synopsys' and Ansys' products across a wide range of EDA and S&A software markets to assess the impact of the Merger. The CMA found that the Merger raises significant competition concerns in three global software markets. The CMA is concerned that the Merger would eliminate competition between two major suppliers that already enjoy strong market positions and exert strong constraints on each other in the following global software markets:

(a) **register transfer level (RTL) power consumption analysis for digital chips**, which is a type of EDA software that is used to check how much power a semiconductor chip consumes and requires to function;

(b) **optics software,** which is a type of S&A software that is used to design and simulate optical systems that manipulate light on a large scale; and

(c) **photonics software**, which is a type of S&A software that is used to design and simulate photonic devices and systems (specifically, to design and simulate nanostructures where it is not appropriate to simplify light as a linear ray).

12. In all of these markets, the CMA found that the Merged Entity would be the clear market leader, and would not face sufficient constraints from remaining competitors post-Merger. The CMA also found that barriers to entry and expansion in these markets are high, in particular because of the high levels of investment in research and development, technical expertise and time required to develop the software. The Merger could therefore result in increased prices and reduced quality and innovation in these markets.

13. Given the Parties' different strengths and inter-relationships across various EDA and S&A markets (with Synopsys primarily active in EDA software and Ansys primarily active in S&A software), the CMA also considered whether the Merger would lead to rivals in various EDA and S&A software markets being harmed as a result of the Merged Entity limiting rivals' access to a key input, reducing or removing interoperability between its products and rivals' products and/or bundling the Parties' tools. Ultimately, however, the CMA considered that the Merged Entity would not have the incentive to engage in this behaviour as the losses of such a strategy would outweigh the gains. In coming to this conclusion, the CMA placed weight on the fact that, amongst other evidence, a significant number of the Parties' top customers – all of whom are sophisticated global companies with extensive industry knowledge – considered that the Merger was unlikely to have such effects. This is because, for example, customers use what they consider to be the best quality software during each stage of their chip design flow (ie they mix and match software from different suppliers) and so interoperability is important to the value of these products, and a significant proportion of customers would switch away from the Merged Entity if interoperability were removed or degraded. The vast majority of customers that responded to the CMA's merger investigation had positive or neutral views on the Merger.

14. Finally, the CMA considered whether the Merger could lead to a loss of future competition between the Parties in the supply of certain S&A software where Synopsys may have entered the market in the future. However, in each of the areas where Synopsys was considering (or had taken steps) to enter, the CMA found that its products would not compete, or would not compete closely, with Ansys' products, which would also continue to face competitive constraints post-Merger.

## What happens next?

15. As a result of these concerns, the CMA believes the Merger gives rise to a realistic prospect of an SLC as a result of horizontal unilateral effects in the supply of the following products globally (i) RTL power consumption analysis for digital chips; (ii) optics software; and (iii) photonics software. The Parties have until 31 December 2024 to offer UILs which might be accepted by the CMA to address the SLCs. If no such UIL is offered, or the CMA decides that any undertaking offered is insufficient to remedy its concerns to the phase 1 standard, then the CMA will refer the Merger for an in-depth phase 2 investigation pursuant to sections 33(1) and 34ZA(2) of the Act.

# ASSESSMENT

## PARTIES, MERGER AND MERGER RATIONALE

### The Parties

16. Synopsys is a global software supplier with two main business segments which are i) design automation, which includes EDA software, services and hardware for designing semiconductors, and ii) design intellectual property (**Design IP**), which refers to IP products in the form of pre-designed building blocks of chip components that can be licensed to customers for use in their chip design processes.[1] Synopsys also supplies optics and photonics software. Synopsys is headquartered in Sunnyvale, California, United States and listed on the Nasdaq Global Select Market.[2] The turnover of Synopsys in 2023 was approximately £4.7 billion worldwide and approximately £[✂] in the UK.[3]

17. ANSYS, Inc. (**Ansys**) is a developer and provider of S&A software and services, which is used to simulate and analyse the behaviour of products, systems or processes via digital models across a wide range of industries including semiconductors, aerospace and defence, automotive, industrial and more.[4] Ansys provides optics and photonics software as part of its S&A activities and also provides EDA software. Ansys is headquartered in Canonsburg, Pennsylvania, United States and listed on the Nasdaq Global Select Market.[5] The turnover of Ansys in 2023 was approximately £1.8 billion worldwide and approximately £[✂] in the UK.[6]

### Merger

18. On 15 January 2024, Synopsys entered into an agreement with Ansys to acquire all the outstanding shares of common stock of Ansys at a total value of approximately $35 billion.[7]

19. The Parties informed the CMA that the Merger is also the subject of ongoing review by competition authorities in the European Union, China, Japan, South Korea, Taiwan, Turkey and the United States.[8]

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[1] Final Merger Notice submitted to the CMA on 22 October 2024 (**FMN**), paragraphs 2.1 and 3.1.
[2] FMN, paragraph 3.1.
[3] FMN, paragraph 6.
[4] FMN, paragraph 3.2.
[5] FMN, paragraph 3.2.
[6] FMN, paragraph 6.
[7] Synopsys' Internal Document, Annex Q7B – 001, 'Execution Copy of Agreement and Plan of Merger by and among Synopsys, Inc., ALTA Acquisition Corp. and Ansys, Inc.', 15 January 2024, page 1; FMN, paragraph 2.32.
[8] FMN, paragraph 2.42. The Parties received unconditional clearance by the Israel competition authority on 9 October 2024.

## Merger rationale

20. The Parties submitted that the main strategic rationale for the Merger is to combine their complementary EDA and S&A businesses to meet customer demand for better integrated solutions.[9] Although the Parties have an existing partnership to offer complementary solutions that began in 2017 and has expanded over time,[10] the Parties submitted that further enhanced integration beyond what is achievable through partnership is necessary to respond to two market trends:

    (a) **Multi-die chips**: the Parties submitted that semiconductor designers have found it increasingly challenging to deliver improvements in computing performance and power efficiency, which has led to the adoption of new innovative design approaches, such as advances in chip architecture. This trend has facilitated the creation of 'multi-die' chips.[11] Since multi-die chips have complex architectures,[12] the design benefits from early and frequent S&A analysis to ensure the chip will perform as expected.[13] In light of the enhanced complexity of the structures, customers need improved design tools that allow engineers to validate design concepts early, reducing the risk of costly iterations later and shortening overall development lead times. Therefore, a deeper integration approach is needed to meet the requirements of customers developing these types of advanced multi-die designs,[14] and the Merger would allow Synopsys to develop more comprehensive and seamless design solutions by combining the Parties' capabilities.

    (b) **Silicon-to-systems**: the Parties submitted that the trend to a 'silicon-to-systems' approach is also driving the need for deeper integration of EDA and S&A software. This approach involves the co-design of semiconductors, hardware, and software of a device and calls for a greater focus on developing, analysing and testing these within the context of the larger systems in which they operate. The increased complexity of the systems within which the chips, hardware and software operate, therefore, necessitates advanced design and testing capabilities (such as the use of 'digital twins').[15]

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[9] FMN, paragraph 2.38.
[10] Ansys | Synopsys Partnership. The partnership encompasses several collaborations. For example, RedHawk SC is offered as an add on to IC Compiler, Synopsys' layout design tool and Synopsys has incorporated limited power integrity analysis capabilities from RedHawk-SC in its digital implementation tools, FMN, paragraphs 7 and 19.18.
[11] FMN, paragraph 2.37.
[12] Multi-die involves assembling different pieces of the chip (also known as 'chiplets' or 'dies') together in a package and connecting them together. Multi-die chips can be assembled as 3D packages, enabling them to exceed the size-limit of 2D designs and deliver higher performance. FMN, paragraph 2.38.
[13] For example, the 'stacking' of components may involve new considerations due to heat dissipation, warping, and cracking of packages due to mechanical stress, while the need for connections between dies may introduce new effects related to noise, spacing rules and mechanical issues. FMN, paragraph 2.37.
[14] FMN, paragraph 2.37.
[15] FMN, paragraph 2.37. A digital twin is a virtual representation of a physical object or system. Digital twins can be used to simulate the behaviour of the object or system to better understand how it will behave in a real-world environment. They can be used by S&A customers to assist with product design and optimize performance. FMN, footnote 8.

21. The CMA considers that the Parties' internal documents broadly support the stated rationale and indicate the importance of greater integration between EDA and S&A tools going forward:

(a) An internal document dated February 2023, setting out Synopsys' strategy in multi-die chip design, states that 'multi-die solution requires comprehensive analysis and integrated analysis-driven exploration and co-optimisation', which is 'a requirement that Synopsys must quickly address in its offering', and acquiring Ansys 'would allow [Synopsys] to expand [✂] and strengthen multi-die position'.[16]

(b) A Synopsys presentation from February 2023 recognises that the multi-die system introduces new challenges, which requires S&A 'early and throughout'. The document considers Synopsys' 'in-design integration' with Ansys as a positive and looks to 'enhance integration' in order to 'extend [✂]' over its competition ([✂]).[17] Another document from around the same time also refers to introducing 'native' S&A solutions for multi-die.[18]

(c) An internal document dated November 2023 describes the 'big megatrends' in the semiconductor industry, including adopting 'multi-die design' and '[s]ilicon to…[s]ystem' paradigm, and that 'multi-die changes takes customer demand for integration to the next level' which requires 'native integration of [Ansys's] multiphysics analysis'.[19]

22. In addition, a number of Synopsys' documents attest to the particular importance of Ansys' S&A products to both its (and, to some extent, its EDA competitors') ability to compete and offer advanced solutions to customers, particularly in the growing multi-die space:[20]

(a) One document from November 2023 characterises both Parties as [✂] (Synopsys in 'accelerating [✂]' and Ansys in '[✂]') and remarks on the need for collaboration between the two companies.[21]

(b) Another Synopsys document from November 2023 refers to how Ansys is relevant to [✂] elements of its strategy developed in 2022 (pre-Merger) including to 'lead in [✂]' where the partnership with Ansys has been [✂] to its [✂]. The document goes on to note that multi-die chip design needs

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[16] Synopsys Internal Document, Annex Q9(SNPS) – 065, '[✂]', February 2023, page 2.
[17] Synopsys Internal Document, Annex Q9(SNPS) – 055, '[✂]', 9 February 2023, pages 4, 8-9.
[18] Synopsys Internal Document, SNPSCMA-00011959, '[✂]', 26 February 2023, slide 3. The Parties submitted that 'native integration' refers to the deepest, broadest and most flexible integration of different capabilities within a single product, that is, the combination of capabilities (as distinct from interoperability between different products). FMN, paragraph 14.37.
[19] Synopsys Internal Document, Annex Q8(SNPS) – 009, '[✂]', 27 November 2023, page 1.
[20] Multi-die is expected to be used in a variety of industries and at the CMA teach-in the Parties explained they expected multi-die chip design to account for around [✂]% of semiconductors, although currently only a small number of customers are active ([✂], [✂] and [✂]). An example of this wider expected adoption is in the mobile market where internal Synopsys documents discuss an '[✂]' and its expectations of '[✂] and [✂] of that segment of [✂] in next [✂] years'. (Synopsys' internal document, Annex SNPSCMA-00011833, '[✂]', 7 August 2022, page 1). Another Synopsys' internal document discusses 'strong adoption' at a number of large customers including [✂] and [✂], among others. (Synopsys' internal document, Annex SNPSCMA-00011959, '[✂]', 26 February 2023, slide 3).
[21] Synopsys' internal document, Annex Q9(SNPS) – 053, '[✂]', 1 November 2023, slide 6.

integrated multi-physics analysis for which it has '[✂]'. This document notes Ansys' key assets as including its [✂] and [✂] products.[22] A different Synopsys document discussing the Merger sees very high value in the integration of its products with these particular Ansys products.[23]

(c) As noted above, the consideration for the Merger is approximately $35 billion, making it one of the largest technology acquisitions of all time. One Synopsys document discussing the financial justification of the Merger notes that 'this [deal] would be a [✂], but if [Ansys] is in fact [✂] to our [✂] in [✂], we must find a way to make the [✂].'

23. The CMA has further considered the Parties' strategic rationale for the Merger where relevant in its competitive assessment.

## PROCEDURE

24. The CMA commenced its phase 1 investigation on 28 October 2024. As part of its phase 1 investigation, the CMA gathered a significant volume of evidence from the Parties. In response to targeted information requests, the CMA received and reviewed internal documents from Synopsys and Ansys to understand the competitive landscape, including but not limited to the Parties' performance and strategy in relation to each of the relevant products. The Parties also had opportunities to make submissions and comment on our emerging thinking throughout the phase 1 investigation. For example, on 26 November 2024, the CMA invited the Parties to attend an Issues Meeting, and the Parties submitted their views in writing. The CMA also gathered evidence from an extensive range of other market participants, such as competitors and customers. The evidence the CMA has gathered has been tested rigorously, and the context in which the evidence was produced has been considered when deciding how much weight to give it.

25. Where necessary, this evidence has been referred to within this Decision.

26. The Merger was considered at a Case Review Meeting.[24]

## JURISDICTION

27. A relevant merger situation exists where arrangements are in progress or contemplation that would lead to two or more enterprises ceasing to be distinct, and either the turnover or the share of supply test is met.

28. Each of Synopsys and Ansys is an enterprise within the meaning of section 129 of the Act. As a result of the Merger, these enterprises will cease to be distinct.

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[22] Synopsys' internal document, Annex Q8(SNPS) – 009, '[✂]', 27 November 2023, page 3. Ansys' RedHawk and HFSS products are discussed further and in more detail in the relevant theories of harm in the competitive assessment.
[23] Synopsys' internal document, Annex Q8(SNPS) – 005, '[✂], 26 October 2023, slide 32.
[24] CMA2, page 39.

Synopsys will acquire all of the outstanding shares of common stock of Ansys, which will result in Ansys being wholly owned by Synopsys.

29. The Parties submitted that the turnover test in section 23 of the Act is not met on the basis that Ansys' UK turnover in 2023 was below £70 million,[25] but that the share of supply test is likely met. The Parties overlap in the supply of both optics software and photonics software, which are each used to design and simulate light-related products globally (including in the UK).[26] The Parties estimated that they have a combined global share of supply of [90-100]% in optics software and [60-70]% in photonics software (with an increment of approximately [40-50]% and [10-20]%, respectively) by value in 2023. The Parties submitted that whilst they have no access to data on supply in the UK specifically, they consider that it is likely that their combined share of supply of each of optics and photonics software in the UK would be above 25%.[27]

30. The CMA has not seen any evidence to indicate that conditions of competition in the supply of optics or photonics software (or the wider supply of EDA and S&A tools) in the UK are materially different to conditions of competition in the supply of these products globally, and therefore considers the global share of supply estimates for the Parties to be a reasonable proxy for the Parties' combined position and the Merger increment in the UK. The Parties operate globally and offer the same products and services across different geographies (including the UK), as do their main competitors.[28] The CMA therefore considers that the share of supply test in section 23 of the Act is met.

31. The CMA therefore believes that it is or may be the case that arrangements are in progress or in contemplation which, if carried into effect, will result in the creation of a relevant merger situation.

32. The initial period for consideration of the Merger under section 34ZA(3) of the Act started on 28 October 2024 and the statutory 40 working day deadline for a decision is therefore 20 December 2024.

## COUNTERFACTUAL

33. The CMA assesses a merger's impact relative to the situation that would prevail absent the merger (ie the counterfactual).[29]

34. In an anticipated merger, the counterfactual may consist of the prevailing conditions of competition, or conditions of competition that involve stronger or weaker competition between the parties to a merger than under the prevailing

[25] FMN, paragraph 6.
[26] The Parties also submitted that they have a global share of over 25% in the supply of EDA tools, with an increment of 3%. FMN, paragraph 5.2 and footnote 62.
[27] FMN, paragraph 5.2.
[28] For that reason and for the avoidance of doubt, where the CMA refers to the global geographic market or effects of the Merger globally throughout the Decision, this includes the UK.
[29] Merger Assessment Guidelines (**CMA129**), March 2021, paragraph 3.1.

conditions of competition.[30] In determining the appropriate counterfactual, the CMA will generally focus on potential changes to the prevailing conditions of competition only where there are reasons to believe that those changes would make a material difference to its competitive assessment.[31]

35. The CMA's conclusion on the counterfactual does not seek to ossify the market at a particular point in time.[32] For example, an assessment based on the prevailing conditions of competition might reflect that, absent the merger under review, a merger firm would have continued making investments in improvements, innovations or new products.

36. The Parties did not submit any alternative counterfactual to the current competitive situation.[33] In this case, the CMA has not received submissions (or other evidence) suggesting that the Merger should be assessed against an alternative counterfactual. Therefore, the CMA considers the prevailing conditions of competition to be the relevant counterfactual. The CMA has taken into account that the prevailing conditions of competition involve an environment where both Parties (and other market participants) are investing and innovating, given the fast-moving nature of these technology markets. The CMA has assessed evidence relating to the Parties' plans in this respect where relevant in the competitive assessment.

# COMPETITIVE ASSESSMENT

## Background and nature of competition

### Industry overview

37. This section provides a high-level overview of the different types of semiconductor chips, the chip design process and an explanation of the software used to design them and how customers procure this software.[34]

*Semiconductor chips*

38. Chips are an important input for electronic devices such as computers, mobile phones and, increasingly, electromechanical / mechanical systems such as automobiles.[35] The main types of chips are:

    (a) **Analog chips** measure and process continuous analog data that comes from real-world signals such as speed, temperature and electrical current. Analog chips are commonly found in electronic devices such as audio equipment,

[30] CMA129, paragraph 3.2.
[31] CMA129, paragraph 3.9.
[32] CMA129, paragraph 3.3.
[33] FMN, paragraph 10.4.
[34] When discussing software for chip design in this Decision, the terms "software" and "tools" are used interchangeably.
[35] FMN, paragraph 14.11.

radio frequency, transceivers, communications, sensors and medical instruments;[36]

(b) **Digital chips**, in contrast to analog chips, process digital signals[37] and can be used for memory, storing data or logic. Digital chips are used in computers and a variety of other digital applications; and

(c) **Mixed-signal chips** include both analog and digital circuits, either to convert a signal from analog to digital (or *vice versa*) or to perform both digital and analog functions. The analog and digital parts of most mixed-signal chips are designed by separate teams.[38]

39. Recent technological advances have also facilitated the creation of new types of chips, notably:

(a) **Photonic chips** which use photons, ie light, instead of electrons to manipulate and transport information. They have a number of advantages over electronic chips, including speed, bandwidth and energy efficiency.[39]

(b) **Multi-die chips**: compared to single-die (ie 2D) chips, these chips can be assembled as 2.5D or 3D packages, enabling them to exceed the size limit of 2D designs and deliver higher performance.[40] Multi-die chips offer significantly improved capabilities and cost benefits and are expected to account for 40% of high-performance chip designs by 2028.[41]

*Chip design flow*

40. Chip design is highly complex and requires a number of different processes before manufacturing begins. There are typically four stages, which are broadly similar for the different types of chips:[42]

(a) **Design:** this stage involves defining the functional behaviour ie technical specification and performance of the chip and forming the building blocks of the chip. As described above in paragraph 15, Synopsys also offers Design IP products with standardised functionality. These products or blocks are licensed to customers that incorporate them in their chip designs so they do not need to develop these independently, thereby reducing costs and time-to-market of the chip.[43]

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[36] FMN, paragraph 14.6.
[37] Ie binary information. FMN, paragraph 14.6.
[38] FMN, paragraph 14.6.
[39] FMN, paragraph 14.8.
[40] There are two principal types of multi-die chips, namely '2.5D ICs', which incorporate two or more chips placed next to each other on the same surface, and '3D ICs', which stack chips on top of each other. FMN, paragraph 14.13-14.14.
[41] FMN, paragraph 10.
[42] FMN, paragraph 14.19. There are some differences specific to each type of chip. Where relevant and to the extent that any differences arise in the design flow for each type of chip, these are discussed in the Competitive assessment section below.
[43] FMN, paragraph 3.1.

(b) **Implementation**: after defining what the chip will do, this stage involves creating and optimising the physical layout of the chip, also referred to as 'physical design';

(c) **Functional verification**: this stage involves tests and analysis to ensure the chip functions according to the intended design; and

(d) **Physical verification and signoff:** in this stage chip designers test the layout to ensure the correct electrical and logical functionality and manufacturability, eg so the chip can operate without overheating, malfunctioning or behaving incorrectly, as well as ensuring that the chip complies with foundry requirements and government regulation.

41. A typical chip design flow will involve between five and twenty EDA and S&A software products, which perform various functions for each step in the chip design process.[44]

*Chip design software products – EDA and S&A*

42. EDA software provides engineers with capabilities to design and validate chips before they are sent to chip manufacturing plants for production (**foundries**).[45]

43. S&A software is also used during the chip design process to *simulate and analyse* the behaviour of a chip via a digital model. Engineers can evaluate alternative designs and explore how their products will react to different situations, including structural, thermal, and optical issues, without the need for a physical prototype.[46]

44. Foundries manufacture chips based on designs provided by chip designers, and certain EDA and S&A software will be certified by foundries to verify the chip design at signoff stage, in line with foundry requirements or government regulations.[47] The CMA heard from third parties that foundry qualification was important. One customer told the CMA its preference was to only design with tools that are certified, and this was especially important for tools at the final physical verification and signoff stages. Foundries are unable to qualify all tools and therefore tools that have been qualified are more likely to be trusted by customers for use in their chip design flows.[48]

45. As noted above in the section on the Merger rationale, the rising demand for advanced high-performance computing chips (such as multi-die chips) in response to customers' evolving requirements has increased the importance of EDA and S&A tools. The substantial resources devoted by each of the Parties to research and development (**R&D**) is also reflective of the growing importance of EDA and S&A. For example, in 2023, Synopsys spent nearly $2 billion (approx. £1.6 billion)

[44] FMN, paragraph 14.20.
[45] Some semiconductor companies manufacture their chips in their own plants, while others rely on foundries (ie companies specialised in manufacturing semiconductors for third parties). FMN, paragraph 14.5.
[46] FMN, paragraph 14.48-14.49.
[47] FMN, paragraph 14.19.
[48] Note of call with a third party, October 2024.

on R&D and its expenditure has consistently increased over the last five years.[49] Ansys's R&D expenditure has also consistently increased over the last five years, with R&D spend in the last year of nearly half a billion ie $495 million (approx. £398 million).[50] As well as investing heavily in R&D, both Parties have undertaken a large number of acquisitions in the EDA (Synopsys) and S&A (Ansys) space in the past two years.[51]

46. Customers of EDA and S&A software include large semiconductor companies, such as Intel, Qualcomm and NVIDIA, which design chips for sale to their customers, as well as large system companies that incorporate chips into their products, such as Apple, Microsoft, Boeing and others.[52] Larger customers tend to procure the 'best-of-breed' software products from multiple vendors and multi-source software products.[53] There are also smaller-sized customers, which tend to make one-off purchases of licences for specific products.[54]

47. Customer evidence shows that customers overwhelmingly consider the quality and technical capabilities of a software product as very important factors when purchasing products. Price, as well as interoperability with other software products, are also both considered very important or important by the vast majority of customers. Other factors, such as whether a supplier offers a portfolio of products or related products, are considered less important, with additional factors such as customer support or a supplier's reputation occasionally mentioned by customers.[55]

48. Interoperability is particularly important to customers as they mix and match software products from different suppliers. There are different ways in which interoperability can be achieved. This includes 'baseline interoperability' which is the use of industry-standard file formats (ie exporting and importing files in the same format across chip design software products).[56] Industry standard file formats are prevalent throughout the industry and suppliers use these industry standard file formats for most software products.[57] Suppliers can also increase interoperability between software products through the use of Application Programming Interfaces (**APIs**),[58] proprietary file formats,[59] and vendor specific

[49] FMN, paragraph 16.2 and 16.3.
[50] FMN, paragraph 16.11.
[51] FMN, paragraphs 4.1-4.3. Synopsys acquired seven EDA businesses in the past two years and Ansys acquired ten S&A businesses in the same period.
[52] FMN, paragraph 14.26.
[53] FMN, paragraph 14.31, as well as evidence received from third parties (Notes of calls with third parties, May and June 2024).
[54] FMN, paragraph 14.226.
[55] Response to the CMA's questionnaire from a number of third parties, October 2024.
[56] Synopsys' submission on interoperability, 8 November 2024, paragraph 2.4 and 3.4.
[57] Note of calls with third parties, June, July, August, and September 2024.
[58] APIs facilitate the flow between different chip design tools where one tool needs to call on another tool, for example, to read or write (ie import or export) a database, file format or to perform a specific function. APIs that call on a tool for a specific function allow the customer to 'call' the function of one tool directly from the interface of other tools. Synopsys' submission on interoperability, 8 November 2024, paragraph 2.10.
[59] Proprietary file formats coexist with industry-file formats and allow suppliers to improve interoperability connection between two chip design tools. In particular, proprietary file formats facilitate the transfer of data between two tools, for example by increasing the transfer speed or reducing storage needs. Synopsys' submission on interoperability, 8 November 2024, paragraph 2.10.

interoperability agreements.[60] Vendor specific interoperability agreements are generally the result of specific requests from customers to facilitate more efficient data interfaces between software products.[61] Synopsys provided evidence showing it had over [✂] vendor specific interoperability agreements with a range of EDA and S&A suppliers including multiple agreements with suppliers such as [✂], [✂], [✂], [✂] and [✂].[62]

49. When asked about their main suppliers of chip design software, customers frequently mentioned four key suppliers – Synopsys, Cadence, Siemens and Ansys.[63] Synopsys and Cadence were generally seen as strong across a range of chip design areas, with Siemens and Ansys seen as strong in particular processes.

## Market definition

50. Where the CMA makes a substantial lessening of competition (**SLC**) finding, this must be 'within any market or markets in the United Kingdom for goods or services'. An SLC can affect the whole or part of a market or markets. Within that context, the assessment of the relevant market(s) is an analytical tool that forms part of the analysis of the competitive effects of the merger and should not be viewed as a separate exercise.[64]

51. Market definition involves identifying the most significant competitive alternatives available to customers of the merger parties and includes the sources of competition to the merger parties that are the immediate determinants of the effects of the merger.[65] While market definition can be an important part of the overall merger assessment process, the CMA's experience is that in most mergers, the evidence gathered as part of the competitive assessment, which will assess the potentially significant constraints on the merger parties' behaviour, captures the competitive dynamics more fully than formal market definition.[66]

### Product market

*Parties' submissions*

52. The Parties submitted that the Merger does not raise competition concerns on any plausible product market and accordingly the market definition may be left open. However, the Parties provided share of supply estimates both for the overall EDA

[60] Vendor specific interoperability agreements allow suppliers to grant each other licences to their software to enable interoperability testing. For example, this could be used in the event a customer experiences a bug and/or requires testing by suppliers to ensure the interoperability connection between tools is seamless in their chip design flows. Synopsys' submission on interoperability, 8 November 2024, paragraph 2.7.
[61] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 7.15.
[62] Synopsys' response to the CMA's Request for Information, 24 May 2024, (RFI 1), Annex RFI1Q25(SNPS)-1.
[63] For example, notes of calls with third parties, May and June 2024.
[64] CMA129, paragraph 9.1.
[65] CMA129, paragraph 9.2.
[66] CMA129, paragraph 9.2.

sector[67] as well as at a more granular product-function level, noting that not all EDA products are substitutable in practice. With respect to specific EDA tools, the Parties submitted that the shares reflect only functional overlaps between the Parties' tools as opposed to defined markets (as some tools are used for multiple functions by different customers).[68] The Parties further submitted that EDA and S&A solutions perform different functions and serve different customer needs.[69] As such, EDA and S&A tools are not typically substitutable and suppliers[70] are generally different across the two segments.[71]

53. The Parties also noted that past decisional practice of the Office of Fair Trading (**OFT**) had considered an overall EDA product market (with potential segmentations by chip design flow stage)[72] and that the European Commission had in *Siemens/Mentor* considered a market for product lifecycle management (**PLM**)[73] and various sub-segments, including EDA, in its competitive assessment, but ultimately left the market definition open.[74] The Parties noted that the European Commission recognised that both customers and competitors consider different EDA software products as complementary rather than substitutable to each other since they provide different functionalities and satisfy different customer needs.[75]

*CMA assessment*

54. The CMA first considered whether it is appropriate to delineate broadly between EDA and S&A software. The CMA considers that while there is some evidence to support such a delineation (with S&A for semiconductor design being one broad use case of a wider portfolio of S&A products that Ansys provides and Ansys being primarily an 'S&A' player and Synopsys being primarily an 'EDA' player), the exact boundaries between the two are not always distinct, and the Parties (as well as Cadence and Siemens) have capabilities across both areas. In addition, as set out in paragraph 58 below the use of S&A in chip design is seen as expanding and 'shifting left'[76] into EDA processes.

[67] Encompassing all tools used for the design, verification, and physical implementation of electronic system, chips and printed circuit boards.
[68] FMN, paragraph 14.84.
[69] FMN, paragraph 14.73.
[70] Other than Cadence and Siemens.
[71] FMN, paragraphs 14.74 and 14.75. For instance, EDA tools are used specifically for the design of semiconductor devices – principally chips, and S&A vendors provide an array of solutions for various processes involved in the design and manufacturing of a broad range of different products.
[72] FMN, paragraph 14.85, referring to Completed acquisition by Synopsys Incorporated of Avant! Corporation, ME/1171/02, 22 August 2002.
[73] The Parties submitted that EDA and S&A sit within the broader 'product lifecycle management' (**PLM**) industry, which comprises all software used to design, simulate and test a product through its lifecycle. (FMN, paragraph 5).
[74] FMN, paragraph 14.86. Siemens/Mentor Graphics, (**Siemens/Mentor**), Case M.83115, 27 February 2017.
[75] FMN, paragraph 14.74. Siemens/Mentor, paragraph 11.
[76] FMN paragraph 16.44-16.47.

*Type of functionality*

55. The CMA also considered whether the relevant product market should aggregate software products offering different functionalities by the Parties into a single EDA and/or S&A market(s), or whether there are separate markets for each type of functionality.

56. The relevant product market is identified primarily by reference to demand-side substitution.[77] The evidence that the CMA has received indicates that from a demand point of view, customers are unable to substitute products with different functionalities across EDA and/or S&A for each other, and that each step of the chip design process relies on different products with a specific use case (as also referred to in the Background and nature of competition section).

57. The CMA heard from third parties that the use case of a specific software product across both EDA and S&A is an important factor when purchasing software products, with one third party stating it is the 'most critical criteria'[78] and another noting that whatever software products it purchases need to fit the specific use case.[79] The Parties' internal documents also often consider segments of EDA and S&A and monitor developments and competitors in different segments separately.[80]

58. Although certain functionalities align to different stages of the chip design flow process (as outlined in the Background and nature of competition section), the boundaries are increasingly blurring with respect to certain functionalities. In particular, the CMA understands that, in response to customer demand, S&A tools that are used later in the chip design flow (ie signoff tools) are increasingly used earlier in the design flow to ensure issues are identified earlier rather than later (when chip layouts are nearly complete and more difficult to change).[81] This is known as 'shift left' and it means that there are some functionalities that are used across different design stages. Therefore, where relevant in its competitive assessment, the CMA has considered the strength of tools across different design stages as an element of differentiation within functionalities rather than defining separate markets within functionalities for each design stage.

59. On the supply-side, the CMA considers that the evidence it has received suggests that suppliers cannot easily adapt a software product designed for one function to perform a different function, as software products are developed to carry out a specific function and require a high level of expertise and R&D investment (both

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[77] CMA129, paragraph 9.7.
[78] Response to the CMA's questionnaire from a third party, August 2024.
[79] Response to the CMA's questionnaire from a third party, August 2024.
[80] Synopsys' Internal Document, Annex Q8(SNPS) - 005, '[✂]', 26 October 2023, slide 6; Synopsys' Internal Document, Annex Q8(SNPS) – 061, '[✂]', 11 June 2023, slide 12; Ansys' Internal Document, Annex s.109(1)(ANSS)-1778, '[✂]', 19 January 2024, slide 2; Ansys' Internal Document, Annex Q9(ANSS) – 022, '[✂]', November 2023, slide 68.
[81] For example, although the Parties have presented transistor-level power integrity analysis as an 'EDA' overlap, the evidence indicates that the boundary with S&A is not clearly delineated. Ansys' Totem(-SC) is fundamentally a signoff tool, but has been introduced at an earlier stage in the design flow and competes with traditional EDA products such as Synopsys' PrimeSim RA. This is one of many examples of Ansys' S&A tools experiencing a "shift-left" in customer demand when designing semiconductor chips. FMN, paragraphs 9, 16.44-16.47, 14.130.

time and cost) to develop, as further discussed below in the Countervailing factors – Entry and expansion section. The CMA also heard that it is extremely difficult to find engineers with expertise to develop certain products, especially in niche areas,[82] and engineers tend to be experts in specific areas,[83] suggesting that the level of expertise and talent required to develop products limits supply-side substitutability.

60. While the main suppliers across the chip design flow (Synopsys, Ansys, Cadence and Siemens) are active across a range of EDA and S&A functionalities, evidence suggests that the competitive landscape differs between functionalities, and across EDA and S&A categories more broadly. Suppliers also have different strengths across different software products, as set out below in the competitive assessment. This is reflected in submissions from the Parties, showing the varying areas of strength of each of the suppliers across a portfolio of over 20 categories of solutions.[84] Evidence from customers also showed that different suppliers have strengths in different functionalities.[85] The competitor set also varies across software products. For example, Ansys only supplies a small number of EDA software products in comparison to Synopsys, and there are a number of small competitors that are active only in the supply of certain software products.

61. Accordingly, the CMA considers that the relevant product markets should be determined based on the functionality of a software product, in particular given evidence of limited demand-side substitutability between different tools across EDA and S&A. The CMA has provided detailed descriptions of what the different functionalities comprise in its discussion of the relevant theories of harm in the competitive assessment below.

*Type of chip*

62. The CMA also considered whether the relevant markets should be segmented based on the type of chip being designed ie between analog, digital, mixed and multi-die chips.

63. While the overall chip design process (as described above in paragraph 40) is similar for different types of chips, the CMA has received evidence that different products are used when designing different types of chips. Some products can only be used for certain types of chip design. For example, Ansys offers different power integrity analysis software products for different types of chips (Ansys' RedHawk-SC is used for digital and multi-die chip design flows whereas Ansys' Totem is used for analog chip design flows only). These products are not substitutable from a customer's perspective as the type of chip they are designing will be determined by the specific project and use of the chip.

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[82] Note of call with a third party, June 2024.
[83] Note of call with a third party, July 2024.
[84] Parties' teach-in presentation to the CMA, dated 29 May 2024, slide 29.
[85] Notes of calls with third parties, June and July 2024.

64. On the supply-side, the CMA has observed differences in the competitor set and competitive strength of suppliers across tools used to design different types of chips. For example, a number of third parties commented on Cadence's strength across the chip design process for analog chips in particular.[86] Ansys, given its strength in S&A, is seen as strong in multi-die design, where S&A analysis is more complex.

65. Accordingly, within functionalities, the CMA has distinguished between different types of chips where relevant (ie, where particular functionality is relevant to more than one type of chip).[87]

*Design IP*

66. The Parties submitted that Design IP products can be segmented by their end use, including into foundation IP products (which are the next level of 'building blocks' above the transistor level) and interface IP products (which allow communication between different chips or parts of chip).[88]

67. The CMA considers that Design IP products could be further segmented into narrower specific end uses (for example, interface IP products can be subdivided by whether the communication is wired or wireless), each of which have distinct use cases and are not demand-side substitutes. Further, competitors have different strengths in each of these narrower sub-categories.[89] As such, the CMA considers that the narrowest relevant markets in Design IP may comprise (i) physical libraries IP, (ii) wired interface IP, and (iii) embedded memories IP. However, ultimately the CMA has left the market definition for Design IP open as the Merger does not raise competition concerns on any basis in relation to Design IP.

## Geographic market

68. The Parties submitted that the appropriate market definition is global on the basis that customers purchase EDA, S&A and Design IP solutions from suppliers irrespective of the suppliers' location and suppliers offer their solutions globally.[90] The Parties also referred to the OFT's decision in *Synopsys/Avant!* which found that the relevant markets for EDA software are international[91] as well as to

[86] Note of a call with a third party, July and September 2024.
[87] The CMA understands that the following relevant functionalities which form the focus of various theories of harm in this Decision are relevant to only one type of chip: RTL power consumption analysis concerns digital chips only; transistor-level power integrity analysis concerns analog chips only; photonic chip simulation and photonic chip layout design implementation tools are each relevant for photonic chips only; and thermal analysis tools relate to multi-die chips only. The CMA considers that distinguishing by chip type is not appropriate for optics or photonics software. The CMA understands that, with regards to chips specifically, photonics software is only relevant for photonic chips, but photonics software has much wider use cases (including simulation of lasers and LEDs) than chips and the CMA has therefore not distinguished by type of chip. Optics software also has a broad use case given it is used to design and simulate optical systems that manipulate light on a large scale, and is not relevant to specific types of chips.
[88] FMN, paragraph 2.1; Annex Q19-002, Synopsys' Design IP Business, 22 October 2024, paragraph 1.1.
[89] Parties' response to the CMA's Request for Information, 14 June 2024, (RFI 2), Annex RFI2Q17.1.
[90] FMN, paragraph 14.90. Final Form CO, Chapter 2, Appendix 2, paragraph 213. Annex Q19-002, FMN, paragraph 2.4.
[91] FMN, paragraph 14.88.

previous practice of the European Commission,[92] which considered that the geographic market for PLM software could be global or at least EEA-wide, although it ultimately left the geographic market definition open.[93]

69. The evidence from the Parties' internal documents[94] and from third parties[95] suggests that the markets for these products are global, with the possible exception of China where different competitive dynamics may apply. The CMA does not consider that the inclusion or exclusion of China would affect its competitive assessment in any event. The CMA has therefore assessed the impact of the Merger globally (including supply in the UK), while leaving open whether China should be included in the relevant markets.[96]

**Conclusion**

70. On the basis of evidence gathered in its investigation, the CMA has assessed the impact of the Merger in the supply of the following products globally:

(a) RTL power consumption analysis for digital chips;

(b) transistor-level power integrity analysis for analog chips;[97]

(c) photonic chip simulation (**PCS**) software for photonic chips;

(d) optics software;

(e) photonics software;

(f) photonic chip layout design (**PLD**) implementation software for photonic chips;

(g) place and route software for digital chips;[98]

(h) place and route software for analog chips;

(i) place and route software for mixed chips;

(j) place and route software for multi-die chips;

(k) circuit simulation software for analog chips;

(l) circuit simulation software for mixed chips;

(m) circuit simulation software for multi-die chips;

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[92] Siemens/Mentor; Dassault/IBM; Siemens/UGS. FMN, paragraph 14.89.
[93] FMN, paragraph 14.89.
[94] For example, Synopsys' internal documents show, among others, that product performance is tracked separately for China and Synopsys entered into a distribution deal for [✂] business. Synopsys' Internal Document, Annex Q9(SNPS) – 035, '[✂]', 1 January 2023; Synopsys' Internal Document, Annex Q9(SNPS) – 038, '[✂]', 1 August 2023, slide 4; Synopsys' Internal Document, Annex Q9(SNPS) – 038, '[✂]', 1 August 2023, slide 55.
[95] Note of a call with a third party, May 2024.
[96] As noted above, where the CMA uses the term 'global' in the Decision it also covers supply in the UK.
[97] The CMA has focused on analog chips but understands that where a mixed chip has an analog component, this tool may also be used.
[98] The CMA understands that within analog and mixed chip design flows P&R tools are often referred to as 'layout' tools.

(n) parasitic analysis software for digital chips;

(o) parasitic analysis software for analog chips;

(p) parasitic analysis software for mixed chips;

(q) parasitic analysis software for multi-die chips;

(r) timing analysis software for digital chips;

(s) timing analysis software for analog chips;

(t) timing analysis software for mixed chips;

(u) timing analysis software for multi-die chips;

(v) gate-level power integrity analysis for digital chips;[99]

(w) gate-level power integrity analysis for multi-die chips;

(x) thermal analysis for multi-die chips;

(y) electromagnetic simulation analysis for analog chips;

(z) electromagnetic simulation analysis for multi-die chips;

(aa) electrostatic discharge (**ESD**) analysis for analog chips;

(bb) ESD analysis for digital chips;

(cc) power device analysis for analog chips; and

(dd) gate-level power consumption analysis for digital chips.

71. The CMA has left open the product market definition for Design IP, but considers that the market is global with the possible exception of China in line with the other products outlined above.

## Theories of harm

72. The CMA assesses the potential competitive effects of mergers by reference to theories of harm. Theories of harm provide a framework for assessing the effects of a merger and whether or not it could lead to an SLC relative to the counterfactual.[100]

73. In its investigation of this Merger, the CMA has considered the following theories of harm:

(a) Theory of Harm 1: Horizontal unilateral effects in the supply of RTL power consumption analysis for digital chips globally;

[99] See FN84 above; the CMA has not focused on mixed chips here, but considers that this tool may also be used in the design of these chips where such a chip has a digital component.
[100] CMA129, paragraph 2.11.

(b) Theory of Harm 2: Horizontal unilateral effects in the supply of transistor-level power integrity analysis for analog chips globally;

(c) Theory of Harm 3: Horizontal unilateral effects in the supply of optics software globally;

(d) Theory of Harm 4: Horizontal unilateral effects in the supply of photonics software globally;

(e) Theory of Harm 5: Horizontal unilateral effects in the supply of PCS software tools for photonic chips globally;

(f) Theory of Harm 6: Vertical effects in the supply of photonic layout design (PLD) implementation software for photonic chips globally;

(g) Theory of Harm 7: Conglomerate effects resulting in the foreclosure of Synopsys competitors by leveraging Ansys' position

(h) Theory of Harm 8: Conglomerate effects resulting in the foreclosure of S&A / EDA software rivals by leveraging Synopsys' position in Design IP globally;

(i) Theory of Harm 9: Loss of future competition in thermal analysis for multi-die chips globally;

(j) Theory of Harm 10: Loss of future competition in electromagnetic simulation analysis for multi-die chips globally; and

(k) Theory of Harm 11: Loss of future competition in gate-level power integrity analysis for multi-die chips globally.

74. Each of these theories of harm is considered below.

**Horizontal unilateral effects**

75. Horizontal unilateral effects can arise in a horizontal merger when one firm merges with a competitor that previously provided a competitive constraint, allowing the merged entity to profitably raise prices or degrade non-price aspects of its competitive offering (such as quality, range, service and innovation) on its own and without needing to coordinate with its rivals.[101] Horizontal unilateral effects are more likely where the merger firms are close competitors or where their products are close substitutes.[102]

76. The CMA has assessed whether it is or may be the case that the Merger may be expected to result in an SLC as a result of horizontal unilateral effects in the following global markets: (i) RTL power consumption analysis for digital chips; (ii) transistor-level power integrity analysis for analog chips; (iii) optics software; (iv) photonics software; and (v) PCS software for photonic chips.

[101] CMA129, paragraph 4.1.
[102] CMA129, paragraph 4.8.

*Theory of Harm 1: Horizontal unilateral effects in the supply of RTL power consumption analysis for digital chips globally*[103]

77. RTL power consumption analysis is a type of EDA software that is used at an early stage of the design process to check how much power a digital chip consumes.[104]

78. The Parties are both active in RTL power consumption analysis through the following products: Synopsys through PrimePower RTL and SpyGlass, and Ansys through PowerArtist.

*Shares of supply*

79. Shares of supply can be useful evidence when assessing closeness of competition. In some cases, such as where the boundaries of the market are not as clear-cut, the CMA may estimate shares of supply but rely to a greater extent on other sources of evidence.[105] In the present case, and as a general point applicable to all theories of harm considered in this Decision, the CMA considers that shares of supply do not provide an accurate indication of a supplier's competitive strength, due to the following limitations:

    (a) some suppliers' software products have multiple use cases across different functionalities, and third parties were not always able to breakdown the revenue of their tools by function. This may result in the revenue attributed to a supplier for a specific product and functionality including revenues generated from that product being used for other functionalities.[106]

    (b) not all suppliers were able to provide comparable breakdowns of revenues by year due to different approaches to the allocation of revenues generated over multi-year licences.

80. More generally, the CMA also considers that a number of the relevant markets considered in this Decision are evolving rapidly and subject to significant technological change, and shares of supply (which provide a historical and static picture of suppliers' positions) may not therefore fully reflect the relative strength posed by suppliers on a forward-looking basis. Therefore, in this context, the CMA has assessed shares of supply alongside other sources of evidence on which it has placed greater weight throughout this Decision.

81. Table 1 sets out the CMA's estimated shares of supply in RTL power consumption analysis globally in 2023.

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[103] See in this respect FN27 above which clarifies that where the CMA refers to effects of the Merger globally, this includes the UK as well.
[104] FMN, paragraph 14.118.
[105] CMA129, paragraphs 4.14-4.15.
[106] FMN, paragraph 14.84. For example, a third party told the CMA that while customers use PowerPro for RTL power consumption analysis, it is also used for gate-level power consumption analysis; Third party response to the CMA's Request for Information, 15 November 2024 (RFI3), paragraph 15.

**Table 1: RTL power consumption analysis (by revenue, global, 2023)**

| Supplier | Share |
|---|---|
| Synopsys | 20-30% |
| Ansys | 20-30% |
| **Combined** | ***40-50%*** |
| Cadence | 10-20% |
| Siemens | 30-40% |
| Magwell | 0-5% |
| **Total** | 100% |

*Source: CMA analysis based on the Parties and competitors' data*[107]

82. Table 1 shows that the Merger would result in the Merged Entity being the largest supplier of RTL power consumption analysis with a combined share of supply by revenue of 40-50% with a significant increment of 20-30%.[108] Siemens (30-40%) and Cadence (10-20%) are the only remaining competitors of any significance, with Magwell having only a minimal presence.[109] The CMA notes that while these shares appear to show that Siemens has a significant market position, this is not supported by the Parties' internal documents or third party views set out in the Alternative constraints section below (and on which the CMA has placed greater evidentiary weight), which indicate that Siemens does not pose a strong constraint on the Parties.

*Closeness of competition*

*Parties' submissions*

83. The Parties submitted that Synopsys and Ansys are not close competitors in this market because Synopsys' PrimePower RTL is more suitable for analyses that require high levels of accuracy and competes with Cadence's Joules RTL, while Ansys' PowerArtist is used for early analyses where speed of analysis is important and competes with Siemens' PowerPro.

[107] FMN, Table 10. Responses to the CMA's questionnaire from a number of third parties, October 2024.
[108] The CMA notes that some third-party estimates indicate the Merged Entity as having an even higher combined share of 89% in 2022; Pedestal Research, 2024.
[109] FMN, Table 10.

*CMA's assessment*

84. The Parties' internal documents indicate that the Parties compete closely and note Ansys' particularly strong market position. Synopsys' internal documents, over the course of several years, reference Ansys' PowerArtist as the [✂] and as a [✂] competitor with [✂] and [✂] to Synopsys' PrimePower RTL and Spyglass.[110] Synopsys' documents also consistently reflect that Synopsys competes with Ansys for [✂] customers (and has [✂] or been [✂] by Ansys' [✂] in relation to several such customers).[111] Similarly, Ansys' internal documents state that Synopsys is a [✂],[112] and competes with Ansys for [✂] customers.[113]

85. The Parties' internal documents do not indicate that any differences between the Parties' software products (having regard to the Parties' submissions on differences in [✂] and [✂]) prevent either Party from viewing the other as a [✂] competitor. The CMA also notes that a greater proportion of Synopsys' revenues in this market are attributable to SpyGlass than to PrimePower RTL, and that the Parties' submission relating to differentiation is not relevant to SpyGlass given the Parties submitted that SpyGlass is used to perform power consumption analysis when high accuracy is *not* required.[114]

86. The feedback received by the CMA from customers also indicates that the Parties compete closely. Approximately half of customers that responded to the CMA's questionnaire noted that the Parties compete closely for RTL power consumption analysis and offer very similar functionality,[115] with one customer noting that it expected PowerArtist to be withdrawn post-Merger as the overlap is high in terms of base features.[116] A minority of customers commented on the relative speed and accuracy of the Parties' offerings, but most did not believe that this was a meaningful source of differentiation.[117]

87. When asked to list providers of RTL power consumption analysis and to rate the strength of the supplier's relevant tool, the majority of third parties that responded rated Synopsys' PrimePower RTL and Ansys' PowerArtist as very strong or strong.[118] The Parties' tools were also mentioned most often, with one third party

[110] Synopsys' Internal Document, SNPSCMA-00011310, '[✂]', 8 August 2022, pages 13 and 14. Synopsys' Internal Document, SNPSCMA-00003401, '[✂]', 20 May 2021, page 47. Synopsys' Internal Document Annex Q9(SNPS) – '[✂]', 1 August 2023, page 33.
[111] Synopsys' Internal Document, SNPSCMA-00001421, '[✂]', 5 March 2023, page 27. Synopsys' Internal Document, SNPSCMA-00001218, '[✂]', 6 April 2023, page 3. Customers include [✂], [✂] and [✂]. Synopsys' Internal Document, SNPSCMA-00003401, '[✂]', 20 May 2021, page 36. Synopsys' Internal Document, SNPSCMA-00005801, '[✂]', 2 January 2022, page 16.
[112] Ansys' Internal Document, Annex s.109(1)(ANSS)-0815, '[✂]', 18 November 2022, page 3.
[113] Ansys' Internal Document, Annex s.109(1)(ANSS)-0889, '[✂]', 27 March 2023, pages 6, 8 and 9. Ansys' Internal Document, Annex s.109(1)(ANSS)-0811, '[✂]', 15 November 2022, page 1.
[114] FMN, paragraphs 14.120, 14.124-14.125.
[115] A number of third parties stated the Parties compete closely. Response to the CMA's questionnaire from a number of third parties, October 2024.
[116] Response to the CMA's questionnaire from a third party, October 2024.
[117] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[118] Ansys; Responses to the CMA's questionnaire from a number of third parties, October 2024; Responses to the CMA's questionnaire from a number of third parties, October 2024.

noting that PrimePower RTL and PowerArtist are the main tools considered by customers when purchasing RTL power consumption analysis tools.[119]

*Alternative constraints*

*Parties' submissions*

88. The Parties submitted that the Merged Entity will face significant competition from both Cadence and Siemens.[120]

*CMA's assessment*

89. As outlined in Table 1, the shares of supply indicate that Siemens and to a lesser extent, Cadence, have material shares (though comparatively smaller than the Parties' combined share). However, the Parties' internal documents and third-party views indicate that both Siemens and Cadence are weak constraints.

90. Synopsys' internal documents consider that Cadence and Siemens have [✂] tools compared to Synopsys and Ansys, which are referenced as '[✂]' and [✂].[121] Ansys' internal documents note that Cadence's Joules and Siemens' PowerPro are [✂] to Ansys' PowerArtist,[122] but are a [✂] constraint than Synopsys, with one 2023 document suggesting that Joules and PowerPro offer [✂] capabilities and functionalities to PowerArtist.[123]

91. The CMA has not seen evidence from the Parties' internal documents of any other competitors or new entrants in the RTL power consumption analysis market.

92. Overall, third parties did not consider there to be strong remaining alternatives to the Parties. The majority of customers rated Cadence's Joules and Siemens' PowerPro as average,[124] with only a few stating they are strong,[125] whereas the majority of customers described PrimePower RTL and PowerArtist as very strong or strong.[126] Both Siemens' and Cadence's competing tools were also mentioned less than the Parties' tools.[127] Third parties also flagged the following limitations of Siemens' and Cadence's tools:

[119] Response to the CMA's questionnaire from a third party, October 2024.
[120] FMN, paragraph 14.127.
[121] Synopsys' Internal Document, Annex Q9(SNPS) - 038- '[✂]', 1 August 2023, page 33. Synopsys' Internal Document, SNPSCMA-00011310, '[✂]', 8 August 2022, page 13.
[122] Ansys' Internal Document, Annex s.109(1)(ANSS)-0811, '[✂]', 15 November 2022, page 1.
[123] Ansys' Internal Document, Annex s.109(1)(ANSS)-0889, '[✂]', March 2023, pages 6, 8 and 9.
[124] Cadence; Responses to the CMA's questionnaire from a number of third parties, October 2024. Siemens; Responses to the CMA's questionnaire from a number of third parties, October 2024.
[125] Cadence; Responses to the CMA's questionnaire from a number of third parties, October 2024. Siemens; Responses to the CMA's questionnaire from a number of third parties, October 2024.
[126] Ansys; Responses to the CMA's questionnaire from a number of third parties, October 2024. Synopsys; Responses to the CMA's questionnaire from a number of third parties, October 2024.
[127] Cadence; Responses to the CMA's questionnaire from a number of third parties, October 2024; Siemens; Responses to the CMA's questionnaire from a number of third parties, October 2024.

(a) One customer said that it decided not to use Cadence's Joules after evaluation, due to very low accuracy.[128]

(b) One customer said that it is reducing the use of Siemens' PowerPro due to issues with power prediction accuracy.[129]

(c) One competitor stated that it does not consider Cadence to be active in the market and that Siemens' PowerPro is the only distant remaining competitor.[130]

93. The vast majority of third parties did not note any other suppliers as being active in the market; of the two additional competitors that were mentioned by one customer, both were rated as only average.[131]

*Conclusion on theory of harm 1*

94. For the reasons set out above, the CMA considers that the Merged Entity would be the largest supplier of RTL power consumption analysis in what is already a concentrated market, and that the Merger would bring about a significant increment of 20-30%. The Parties are market leaders and close competitors, offering tools with similar functionality and capabilities. Only two other competitors – Cadence and Siemens – remain, and these impose a weak constraint (both individually and in aggregate).

95. Accordingly, the CMA found that the Merger raises significant competition concerns as a result of horizontal unilateral effects in the supply of RTL power consumption analysis globally.

*Theory of Harm 2: Horizontal unilateral effects in the supply of transistor-level power integrity analysis for analog chips globally*

96. The Parties are both active in transistor-level power integrity analysis; Synopsys through PrimeSim RA and Ansys through Totem. Power integrity analysis is a type of software that checks a chip's reliability when using power to ensure it will continue to function correctly. This analysis is typically done at the final signoff stage of the chip design flow but can also be used at an earlier design stage to pre-empt power integrity issues.[132] Analysis can be run at both transistor and gate-level with transistor-level analysis used mostly for analog chips.[133]

[128] Response to the CMA's questionnaire from a third party, October 2024.
[129] Response to the CMA's questionnaire from a third party, October 2024.
[130] Response to the CMA's questionnaire from a third party, October 2024.
[131] Response to the CMA's questionnaire from a third party, October 2024.
[132] See also footnote 81.
[133] FMN, paragraphs 14.128-14.129.

*Shares of supply*

97. Table 2 sets out the CMA's estimated shares of supply in transistor-level power integrity analysis in 2023.[134]

**Table 2: Transistor-level power integrity analysis (by revenue, global, 2023)**

| Supplier | Share, 2023 |
|---|---|
| Synopsys | 5-10% |
| Ansys | 60-70% |
| ***Combined*** | ***70-80%*** |
| Cadence | 10-20% |
| Siemens | 5-10% |
| Empyrean | 5-10% |
| **Total** | **100%** |

*Source: CMA analysis based on the Parties and competitors' data*[135]

98. Table 2 shows that Ansys has a strong market position (60-70%), with Cadence (10-20%) as the next largest supplier, and Synopsys (5-10%), Siemens (5-10%) and Empyrean (5-10%) having notably smaller shares.

*Closeness of competition*

*Parties' submissions*

99. The Parties submitted that Synopsys and Ansys are both active in the supply of transistor-level power integrity analysis but that they are not close competitors on the basis that:

(a) The Parties' tools are complementary and face different competitors.[136] Synopsys' PrimeSim RA focuses primarily on reliability and robustness analysis (which represents a different market),[137] whereas Ansys' Totem focuses specifically on transistor-level power integrity analysis;[138]

[134] FMN, Table 11.
[135] FMN, Table 11. Responses to the CMA's questionnaire from a number of third parties, October 2024. The CMA did not receive third party evidence from one competitor and has supplemented with the Parties' estimation.
[136] The Parties submitted that Synopsys' PrimeSim RA competes with Siemens' Solido and DefectSim and Cadence's Legato and RelXpert whereas Ansys' Totem competes with Cadence's Voltus-FI, Siemens' mPower Analog and Empyrean's Patron. Parties' additional response to the Issues Letter, 27 November 2024, paragraph 3.3.
[137] Reliability and robustness analysis tools predict how devices can alter their behaviour during their lifetime while transistor-level power integrity tools are used to detect unwanted voltage drops. Third party response to the CMA's follow-up questions regarding Request for Information, 3 December 2024, paragraph 2.
[138] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 3.3.

(b) Synopsys' PrimeSim RA lacks several advanced features of Ansys' Totem and is unable to match capacity and performance levels required for transistor-level power integrity analysis;[139] and

(c) PrimeSim RA has limited use cases and is often used in smaller designs or by memory chip companies, whereas Totem is the tool of choice for leading semiconductor companies for large designs.[140]

100. The Parties also submitted that the minimal increment provided by Synopsys would not have a material impact on the current competitive landscape.[141]

*CMA's assessment*

101. The CMA does not consider the Parties' submission that Synopsys' PrimeSim RA offers broader capabilities in reliability and robustness analysis as well as transistor-level power integrity analysis to be relevant to its assessment of closeness of competition between the Parties' products in the market for transistor-level power integrity analysis specifically. Within the relevant transistor-level power integrity analysis market, however, the CMA has not seen evidence to indicate that the Parties' products compete closely, with some feedback to support the Parties' submission that PrimeSim RA is primarily a reliability and robustness analysis software product and is a weak product in the market for transistor-level power integrity analysis.

102. The evidence in the Parties' internal documents and from third parties broadly reflects the market positions presented in Table 2: namely that Ansys is a strong and leading supplier, with Synopsys having a much weaker market position. A 2024 Ansys internal document lists Synopsys' PrimeSim RA as a competitor to Ansys' Totem for transistor-level power integrity analysis but shows PrimeSim RA as having a [✂] overlap with Ansys' Totem that is also [✂] than the overlap between Ansys' Totem and Cadence's Voltus-Fi/XFi, Siemens' mPower Analog and Empyrean's Patron. No [✂] are listed for PrimeSim RA; instead, Ansys notes that it has [✂] features and does not have a [✂] user interface.[142] One Synopsys internal document shows that it recommended the use of Ansys' [✂] to [✂] for transistor-level power integrity analysis (as opposed to [✂] software product).[143] Further, the CMA has not seen any evidence in Synopsys' documents of customers switching from Synopsys' PrimeSim RA to Ansys' Totem or vice versa.[144]

[139] FMN, paragraph 14.133. Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 3.3.
[140] FMN, paragraph 14.134. Parties' response to the CMA's Issues Letter, 27 November 2024, paragraph 3.3.
[141] FMN, paragraph 14.132. Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 3.2.
[142] Ansys' Internal Document, Annex s.109(1)(ANSS)-2117, '[✂]', 26 February 2024, page 3.
[143] Synopsys' Internal Document, SNPSCMA-00010638, '[✂]', 6 February 2024, page 5.
[144] Synopsys' Internal Document, SNPSCMA-00001451, '[✂]', 7 May 2024, page 7; Synopsys' Internal Document SNPSCMA-00001373, '[✂]', 4 March 2023, page 5; Synopsys' Internal Document, SNPSCMA-00001321, '[✂]', 10 September 2024, page 9.

103. The vast majority of customers did not consider that the Parties compete closely, with over half noting that they did not consider Synopsys to be active in the supply of transistor-level power integrity analysis.[145]

104. Third parties mentioned Ansys' Totem most frequently when asked about transistor-level power integrity analysis software products that meet their requirements[146] and consistently referred to it as the long-established industry-leading software product,[147] closely followed by Cadence's Voltus-FI.[148] In contrast, Synopsys' PrimeSim RA was only mentioned by a minority of third parties and was generally rated by those third parties as average (as opposed to strong or very strong like Ansys' Totem).[149] While one competitor noted that Synopsys' PrimeSim RA was gaining traction,[150] several customers (that regarded Synopsys as being active in the market) indicated that Synopsys' PrimeSim RA is not an alternative to Ansys' Totem on the basis that PrimeSim RA, in line with the Parties submissions, can only be used for small-sized designs; [151] is used for a different purpose (dynamic analysis) to Ansys' Totem's special processing functions within this market;[152] and more generally, that PrimeSim RA's adoption rate across the market is low.[153]

105. In all instances where a customer rated Synopsys' PrimeSim RA as stronger than average, Ansys' Totem was not mentioned as an alternative transistor-level power integrity analysis software product, indicating a lack of substitutability for the customer's specific requirements.[154]

*Alternative constraints*

*Parties' submissions*

106. The Parties submitted that the Merged Entity would face significant competition from Cadence, which they submitted was the historic market leader, certified by several large foundries and offering advanced features. The Parties further submitted that (i) Siemens is a new and rapidly growing market entrant having recently acquired foundry certification,[155] and Ansys' customers have recently

[145] Response to the CMA's questionnaire from a number of third parties, October 2024.
[146] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[147] With customers referencing Totem as 'industry benchmark'; 'the first player to enter the market' and 'de facto standard'. Responses to the CMA's questionnaire from a number of third parties, October 2024.
[148] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[149] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[150] Response to the CMA's questionnaire from a third party, October 2024.
[151] Response to the CMA's questionnaire from a third party, October 2024.
[152] Response to the CMA's questionnaire from a third party, October 2024.
[153] Response to the CMA's questionnaire from a third party, October 2024.
[154] Response to the CMA's questionnaire from a number of third parties, October 2024.
[155] The Parties submitted that Synopsys' PrimeSim transistor-level power integrity analysis functionality was developed in 2004 and received foundry certification in 2015. Siemens' mPower entered in 2019 and received foundry certification in 2021 and is therefore expected to grow. Parties' response to the CMA's RFI 10, paragraph 2.1. Parties' additional response to the Issues Letter, 27 November 2024, paragraph 3.6.

switched away to Siemens,[156] and (ii) Empyrean is also a recent and fast-growing market entrant.[157]

*CMA's assessment*

107. The evidence in the Parties' internal documents and from third parties indicates that Cadence's Voltus-FI/XFI is the primary competitive constraint on Ansys in this market, and a much stronger constraint on Ansys than suggested by the CMA's shares of supply estimates in Table 2.

108. An Ansys internal document from 2024 which sets out the competitive landscape for Totem in transistor-level power integrity analysis shows Cadence's Voltus-FI/XFI as the [✂] competitor with the [✂] overlap with Ansys' Totem.[158] This is also consistent with other Ansys internal documents which show that it monitors and benchmarks Totem against Cadence's foundry-certified Voltus-FI product[159] (conversely, the CMA has not seen similar evidence for Synopsys' PrimeSim RA). When asked about the options and strength of suppliers for transistor-level power integrity analysis, customers mentioned Cadence's Voltus FI/XFI approximately the same number of times as Ansys' Totem and it was generally rated by customers as a strong software product.[160] Several customers identified it as a strong alternative to Ansys' Totem and noted that it also benefits from close integration into Cadence's other software products,[161] although some customers said it has weaknesses in comparison to Ansys' Totem.[162] One customer stated that the Parties do not compete closely as Cadence is the main supplier in this market.[163]

109. An Ansys internal document which sets out the competitive landscape for transistor-level power integrity analysis shows both Siemens' mPower and Empyrean's Patron [✂] with Ansys' Totem to a [✂] extent than Synopsys' PrimeSim RA, although both are described as 'not yet [✂] (or [✂]) by [✂] customers'.[164] There is also evidence of Siemens' mPower competing with Ansys' Totem for the same customers,[165] and that Ansys considers that Siemens is becoming 'more [✂] in this area'.[166] Third parties identified Siemens' mPower's

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[156] Parties' response to the [✂] Request for Information, 3 December 2024, paragraph 1.13.
[157] FMN, paragraph 14.135. Parties' response to the Issues Letter, 27 November 2024, paragraph 3.6.
[158] Ansys' Internal Document, Annex s.109(1)(ANSS)-2117, '[✂]', 26 February 2024, page 3.
[159] Ansys' Internal Document, Annex s.109(1)(ANSS)-0718, '[✂]',11 July 2022, pages 7-10; Ansys' Internal Document, Annex s.109(1)(ANSS)-0904, '[✂]', 21 April 2023, page 55. See: https://www.cadence.com/en_US/home/company/newsroom/press-releases/pr/2022/samsung-foundry-certifies-cadence-voltus-xfi-custom-power.html and https://www.cadence.com/en_US/home/tools/digital-design-and-signoff/silicon-signoff/voltus-fi-custom-power-integrity-solution.html.
[160] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[161] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[162] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[163] Response to the CMA's questionnaire from a third party, October 2024.
[164] Ansys' Internal Document, Annex s.109(1)(ANSS)-2117, February 2024, page 3.
[165] Annex RFI 25 Q 1.2 to the Parties' response to the [✂] Request for Information, 3 December 2024, 28 September 2021, page 1; Annex RFI 25 Q 1.4 to the Parties' response to the [✂] Request for Information, 3 December 2024,18 December 2023, page 4.
[166] Annex RFI 25 Q 1.2 to the Parties' response to the [✂] Request for Information, 3 December 2024, 28 September 2021, page 1.

foundry-certified product less frequently than Ansys' Totem but more often than Synopsys' PrimeSim RA, and the majority rated it as average.[167] One customer described it as adequate, but noted that some of Synopsys' PrimeSim RA advanced functions were inferior to Ansys' Totem.[168]

110. The CMA did not see any evidence from either the Parties' internal documents or third party views to support the Parties' submission that Empyrean (which is currently foundry certified in China)[169] is a growing constraint on the Merged Entity. The CMA also saw limited evidence of any other competitors exerting a material constraint, although one competitor stated that it had recently entered a segment of the market for transistor-level power integrity analysis and is developing a second product. It rated its current offering as average.[170]

*Conclusion on theory of harm 2*

111. For the reasons set out above, the CMA considers that while Ansys has a strong market position, Synopsys is a weak competitor that does not exert any meaningful constraint on Ansys. The Merged Entity would continue to face a strong constraint from Cadence, alongside several smaller existing and expanding competitors.

112. Accordingly, the CMA found that the Merger does not give rise to a realistic prospect of an SLC as a result of horizontal unilateral effects in the supply of transistor-level power integrity analysis globally.

*Theory of Harm 3: Horizontal unilateral effects in the supply of optics software globally*

113. Optics software forms part of the broader S&A space and is used for the design and simulation of optical products (specifically, to design and simulate systems that manipulate light on a macro scale, primarily using raytracing technology).[171]

114. The Parties are both active in the supply of optics software through a number of marketed as well as pipeline software products and services. Synopsys' Optical Solutions Group (**OSG**) offers a number of solutions (CODE V, LightTools, and LucidShape),[172] provides optical services, namely Optical Engineering Services, Optical Scattering Measurements and Equipment and ImSym;[173] and has [✂] new products in its development pipeline ([✂] to [✂] and [✂], and [✂]).[174] Ansys

[167] Responses to the CMA's questionnaire from a number of third parties, October 2024. https://newsroom.sw.siemens.com/en-US/mpower-tower-ic-design/
[168] Response to the CMA's questionnaire from a third party, October 2024.
[169] Parties' response to the CMA's Issues Letter, 27 November 2024, footnote 10.
[170] Response to the CMA's questionnaire from a third party, October 2024.
[171] FMN, paragraph 14.301.
[172] FMN, paragraph 14.312.
[173] FMN, paragraph 14.313.
[174] FMN, paragraph 14.314.

offers two optics software solutions (Zemax and Speos),[175] and earlier this year, it also announced a partnership with DXOMARK for a pipeline product.[176]

*Shares of supply*

115. The Parties' estimated shares for optics software (based on global revenues) indicate that in 2023 the Parties' combined share of supply was [90-100]% (with a very high increment of [40-50]% as a result of the Merger), suggesting that post-Merger, the Merged Entity would capture the [✂] market of optics software. The lack of any constraints on the Merged Entity reflected in these shares of supply is also consistent with the Parties' internal documents and third-party feedback, as discussed further below. The CMA considers that the shares of supply suggest that the Parties are close competitors to each other given the absence of any alternatives, and therefore raise *prima facie* competition concerns.

*Closeness of competition*

*Parties' submissions*

116. The Parties submitted that although their solutions overlap, they have different focus areas.[177] Where customers use both Parties' software, it is because they want the best-of-breed solution for different functionalities. The Parties also submitted that although Synopsys' CODE V competes with Ansys' Zemax, Ansys' Zemax has additional functionality that Synopsys' CODE V lacks.[178]

*CMA's assessment*

117. At the outset, the CMA notes that the Parties' [90-100]% combined share of supply already indicates that the Parties are, by definition, each other's closest competitor. This is confirmed by the Parties' internal documents, which indicate that the Parties view each other as close competitors in the supply of optics software and acknowledge the very limited competitive constraint from other rivals. For example, internal documents show that Synopsys views Ansys' campaigns for Speos as the '[✂]' to its LightTools and LucidShape software products,[179] and that Ansys views Synopsys as its '[✂] competitor'.[180]

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[175] FMN, paragraph 14.316.
[176] FMN, paragraph 14.317.
[177] The Parties explained that Synopsys' LucidShape and LightTools compete with Ansys' Speos. However, Ansys' Speos is predominantly a visualisation tool, with a secondary raytracing functionality, whereas Synopsys' tools would be favoured by customers who want a stronger raytracing tool and have less need for visualization. The Parties further submitted that Ansys' Speos competes more closely with other visualization tools such as Autodesk VRED and companies such as NVIDIA. FMN, paragraph 14.323.
[178] FMN, paragraph 14.323.
[179] Synopsys' internal document, Annex SNPSCMA-00001064, '[✂]', 12 February 2022, slides 14-18. The same document shows Synopsys monitoring Ansys' investment in optics over the past [✂] years.
[180] Ansys' Internal Document, Annex s.109(1)ANSS–1356, '[✂]', 17 November 2023, slide 20. While Ansys acknowledges the presence of competitors in the supply of the different optics products, it considers Synopsys' LucidShape and LightTools as having '[✂]' of the market.

118. Third parties also told the CMA that Synopsys and Ansys compete closely in optics software and that there are very limited competitive constraints on the Parties. For example, customers told the CMA that the Parties are the only two suppliers of optics software products,[181] that the main overlap between Synopsys and Ansys software products is in the optics space,[182] and that Synopsys' Code V/LightTools compete closely with Ansys' Zemax.[183] One competitor told the CMA that competition in this segment takes place among a 'very limited' number of vendors, with Synopsys and Ansys being the 'key players'.[184]

*Alternative competitive constraints*

*Parties' submissions*

119. The Parties submitted that despite their high combined share, they face competition from numerous competitors including smaller rivals, namely Breault Research Organisation, COMSOL Multiphysics, Lambda Research Corporation, LightTrans and Silvaco, as well as competition from disruptive entrants, such as Quadoa Optical Systems and Photon Engineering.[185]

120. The Parties also submitted that they face competition from in-house solutions which may be used by manufacturers of optical systems. For example, many of the Parties' largest customers, such as [✂], [✂], [✂] and [✂] have in-house tools and may sometimes only purchase the Parties' tools to benchmark their own tools' functionalities.[186]

*CMA's assessment*

121. The Parties' internal documents in relation to optics software contain very limited reference to competitors (other than the Parties themselves), and do not show that the Parties regard potential new entrants as a competitive threat.

122. Third parties indicated that there are very limited competitive constraints on the Parties. As stated above in paragraph 118, customers indicated that the Parties are the only two suppliers of optics software. One third party told the CMA that post-Merger only a limited number of very small competitors will remain, each with a share that is only a fraction of the Merged Entity's. The same third party told the CMA that none of the smaller competitors can provide the same solutions at scale or the same support to customers as Synopsys and Ansys, and that it would take years for another fully capable alternative solution to theoretically become available in the market.[187]

[181] Note of a call with a third party, June 2024.
[182] Note of a call with a third party, June 2024.
[183] Response to the CMA's questionnaire from a third party, August 2024.
[184] Submission to the CMA from a third party, April 2024.
[185] FMN, paragraph 14.324.
[186] FMN, paragraph 14.325.
[187] Submission to the CMA from a third party, April 2024.

123. When third parties were asked to indicate the names of Synopsys' and Ansys' tools or products for which they considered there were no good alternatives, one third party identified Ansys' Zemax and Speos as well as Synopsys' CODE V, LightTools and LucidShape,[188] while another referred to Ansys' optics tools as quite advanced when compared to alternatives.[189] The CMA did not receive any evidence from customers indicating that there are credible alternatives to the Parties or that in-house solutions were an alternative to the tools offered by the Parties.

*Conclusion on theory of harm 3*

124. For the reasons set out above, the CMA believes that the Parties have a very high combined share of supply and compete closely and that other competitors do not exert any competitive constraint on the Parties.

125. Accordingly, the CMA found that the Merger raises significant competition concerns as a result of horizontal unilateral effects in the supply of optics software globally.

*Theory of Harm 4: Horizontal unilateral effects in the supply of photonics software globally*

126. Photonics software forms part of the broader S&A space and is used for the design and simulation of photonic devices and systems (specifically, to design and simulate nanostructures where it is not appropriate to simplify light as a linear ray).[190]

127. Synopsys and Ansys are both active in the supply of photonics software through their respective software products, namely RSoft and Lumerical.[191]

*Shares of supply*

128. The Parties' estimated global shares for photonics software (based on global revenues) indicate that in 2023 the Parties' combined share was [60-70]%. Post-Merger, the Merged Entity would be the largest supplier of photonics software with a material increment of [10-20]% arising as a result of the Merger. The only competition the Merged Entity would face post-Merger would be from a long tail of smaller suppliers.[192] The absence of meaningful competitive constraints is reflected in the Parties' internal documents and third-party evidence, as discussed further below. The CMA considers that the shares of supply, despite the general

[188] Response to the CMA's questionnaire from a third party, August 2024.
[189] Response to the CMA's questionnaire from a third party, August 2024.
[190] FMN, paragraph 14.301.
[191] Synopsys' OSG offers a photonics solution, namely RSoft, which is a portfolio of photonic simulators. RSoft comprises a core design (3D CAD) module and several simulation modules. Ansys offers Lumerical, which is also a portfolio of photonic simulators integrated with a 3D CAD design environment. FMN, paragraphs 14.318-14.319.
[192] The Parties did not submit any estimates for competitors' revenues for this overlap but indicated that the Parties would face a tail of smaller competitors.

limitations set out above, provide a strong indication that the Parties are significant alternatives to each other.

*Closeness of competition*

*Parties' submissions*

129. The Parties acknowledged that their respective RSoft and Lumerical software products are overlapping solutions, which provide similar functionality and compete against each other.[193]

*CMA's assessment*

130. The Parties' internal documents indicate that the Parties view each other as close competitors in the supply of photonics software. For example:

(a) One Synopsys document refers to and monitors the investments made by Ansys over the past [✂] years in the optics and photonics segment, which it considers by far its '[✂]'[194] and in the same document refers to its aim to get [✂]% of Ansys' [✂] to [✂] to Synopsys' [✂].[195] Another document also refers to evidence of [✂] between Synopsys' RSoft and Ansys' Lumerical.[196]

(b) Similarly, while Ansys considers its product a '[✂]' and 'preferred partner' in the photonics software market,[197] its documents also acknowledge that Synopsys has a long history in photonics.[198]

131. Third parties indicated that Synopsys and Ansys compete closely in the supply of photonics software and there are very limited competitive constraints on the Parties. For example, one customer told the CMA that the Parties' products compete closely, and that many functionalities of RSoft and Lumerical are the same.[199]

*Alternative competitive constraints*

*Parties' submissions*

132. The Parties submitted that despite their high combined share of supply, they face competition from multiple smaller competitors, namely VPIphotonics, Photon Design, FlexCompute, COMSOL Multiphysics, CrossLight Software, Fluxim, JCM and Optiwave Systems.[200] The Parties further submitted that they also face

[193] FMN, paragraph 14.327.
[194] Synopsys' internal document, Annex SNPSCMA-00001221, '[✂]', 10 July 2023, slide 8.
[195] Synopsys' internal document, Annex SNPSCMA-00001221, '[✂]', 10 July 2023, slide 13 and slide 15.
[196] Synopsys' Internal Document, Annex SNPSCMA-00001221, '[✂]', 6 July 2023, slides 13 and 15.
[197] Ansys' Internal Document, Annex s.109(1)(ANSS)-1079, '[✂]', 25 September 2023, slide 59.
[198] Ansys' internal document, Annex Q9(ANSS) - 042, '[✂]', April 2022, slide 2.
[199] Response to the CMA's questionnaire from a third party, August 2024.
[200] FMN, paragraph 14.328.

competition from in-house solutions, which the largest customers are able to develop.[201]

*CMA's assessment*

133. The Parties' internal documents in relation to photonics software contain very limited reference to competitors (other than the Parties themselves), and do not indicate that the Parties consider the potential new entrants as a competitive threat.

134. As stated above in paragraph 131, third party evidence indicates a lack of competitive constraints on the Parties. One third party stated that although there are alternative providers to Ansys and Synopsys, they are not yet viewed as commercially viable and/or often depend on Ansys' Lumerical for interoperability. The same third party also stated that entry into this category is difficult given the significant time and cost requirements associated with developing new code.[202]

135. When third parties were asked by the CMA for the names of any Synopsys or Ansys products for which they considered there were no good alternatives, one customer indicated that post-Merger it was 'not sure how many [other] good tools are out there' for physical simulation of photonic components.[203] Moreover, the CMA did not receive any evidence from customers indicating that there are credible alternatives to the Parties or that in-house solutions were an alternative to the tools offered by the Parties.

*Conclusion on theory of harm 4*

136. For the reasons set out above, the CMA believes that the Parties have a very high combined share of supply, that they compete closely and that competitors do not exert any meaningful competitive constraint over the Parties.

137. Accordingly, the CMA found that the Merger raises significant competition concerns as a result of horizontal unilateral effects in the supply of photonics software globally.

*Theory of Harm 5: Horizontal unilateral effects in the supply of PCS software tools for photonic chips globally*

138. The Parties are both active in the supply of photonic chip simulation (PCS) software: Synopsys through OptSim, and Ansys through Lumerical Interconnect. PCS software allow designers to simulate and analyse the behaviour of a photonic chip to predict and verify the chip's performance.[204]

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[201] FMN, paragraph 14.329.
[202] Submission to the CMA from a third party, April 2024.
[203] Response to the CMA's questionnaire from a third party, August 2024.
[204] FMN, paragraph 14.183.

*Parties' Activities*

139. Synopsys' OptSim and Ansys' Lumerical Interconnect are both upstream inputs to photonic chip layout design implementation software (or PLD implementation software, as defined in paragraph 70(f), which allow designers to create the layout of a photonic chip). At the downstream PLD level, Synopsys is active through OptoCompiler where it competes with several other suppliers of PLD implementation software. Ansys is not active downstream in PLD implementation software, but it supplies Lumerical Interconnect as PCS software to customers for use as an input into PLD implementation software supplied by third parties (provided these interoperate with Lumerical Interconnect). Examples of PLD implementation software that customers can use Lumerical Interconnect with include Cadence's Virtuoso and Siemens' L-Edit, both of which compete with Synopsys' OptoCompiler. The vertical relationship between the Parties in this respect is considered in Theory of Harm 6: Vertical effects in the supply of photonic layout design (PLD) implementation software for photonic chips globally.

*Parties' submissions*

140. The Parties submitted that Synopsys and Ansys are not close competitors in the supply of PCS software as competition takes place at the downstream level for PLD implementation software and the choice of PCS software is secondary. They submitted that customers choose a PCS software that works with the PLD implementation software of their choice. They may buy both types of software from the same supplier or different suppliers (provided the software interoperate). Accordingly, the Parties have different areas of focus:

    (a) Synopsys focuses on sales of its PLD implementation software, OptoCompiler, and does not actively pursue OptSim-only opportunities upstream at the PCS level; and

    (b) Ansys focuses on its sales of Lumerical Interconnect to customers that have already purchased PLD implementation software from one of Synopsys' downstream competitors such as Cadence and Siemens.[205]

141. The Parties further submitted that not all customers use PCS software during their chip design process.[206]

*CMA's view on the Parties' Activities*

142. The CMA considers that the Parties compete in the supply of PCS software as Synopsys sells OptSim on a standalone basis[207] as well as selling its integrated photonic design flow (PCS + PLD). Ansys only offers its PCS software on a

[205] FMN, paragraphs 14.123-14.124
[206] FMN, paragraph 14.123.
[207] FMN, paragraph 14.200; Annex RFI4Q5.1 to the Parties' response to the CMA's RFI4, August 2024.

standalone basis for use with third party PLD implementation software, as it does not offer a full photonic design flow.[208]

143. The CMA considers that PCS software is currently important to some customers designing and simulating a photonic chip, and that competition does not solely occur at the PLD implementation software level (ie with the choice of PLD implementation software in effect determining the choice of PCS software). In particular, the majority of customers told the CMA that:

(a) they require PCS software to design a photonic chip;[209] and

(b) they consider/purchase PCS software alongside PLD implementation software.[210]

144. Based on the evidence above, the CMA considers that Synopsys' OptSim and Ansys' Lumerical Interconnect compete at the PCS software level and that evidence on customer purchasing behaviour indicates that it is appropriate to assess whether it is or may be the case that the Merger may be expected to result in an SLC as a result of horizontal unilateral effects in the supply of PCS software globally.

*Shares of supply*

145. Table 3 sets out the CMA's estimated shares of supply in PCS software in 2023 based on the Parties' and competitors' submissions.

[208] Ansys' Internal Document, Annex s.109(1)(ANSS)-1115, '[✂]', 13 October 2023, page 27.
[209] Response to the CMA's questionnaire from a number of third parties, October 2024.
[210] Response to the CMA's questionnaire from a number of third parties, October 2024.

**Table 3: Photonic chip simulation software (by revenue, global, 2023)**

| Supplier | Share |
|---|---|
| Synopsys | 10-20% |
| Ansys | 40-50% |
| ***Combined*** | ***50-60%*** |
| VPI Photonics | 30-40% |
| Photon Design | 5-10% |
| Total | 100% |

*Source: CMA analysis based on the Parties' estimates and competitors' data*[211]

146. Table 3 shows that Ansys has a strong market position in PCS software with a share of 40-50%, with VPI Photonics as the next largest competitor. Synopsys has a lower share (10-20%)%[212] and Photon Design has a notably smaller share. However, in addition to the general limitations of relying on shares of supply in these types of markets (as outlined in paragraphs 79 and 80), the CMA considers there to be significant limitations to this dataset:

(a) First, several competitors are unaccounted for. The CMA understands that both Luceda[213] and OptiWave are active in the supply of PCS software; however, the CMA did not receive data from these third parties, and the Parties did not provide share of supply estimates for them.[214]

(b) Second, the shares of supply do not account for the increasing constraint posed by combinations of a 'Verilog-A' model and electrical simulators offered by Cadence and others (which are discussed further below in the section on Alternative constraints).

[211] FMN, Table 18. Response to the CMA's questionnaire from a third party, October 2024. The CMA did not receive third party evidence from a competitor and, for this competitor, has therefore used the Parties' estimates, where possible.
[212] This includes total revenues for OptSim (ie customers that purchase OptSim and OptoCompiler and those that purchase OptSim for use with another PLD implementation software).
[213] The CMA understands that Luceda offers its PCS software primarily as part of an integrated offering with its PLD implementation software, IPKISS. One third party told the CMA that its PLD implementation software interoperates with Luceda's PCS software. Response to the CMA's questionnaire from a third party, October 2024.
[214] The CMA did not receive third party evidence from a competitor and has therefore used the Parties' estimates, where possible. The CMA has not included revenue estimates for electrical simulators Cadence's Spectre or Keysight's ADS as it has considered these as part of future developments ongoing in the industry, as considered later on in this theory of harm. FMN, Table 18. Response to the CMA's questionnaire from a third party, October 2024.

*Closeness of competition*

*Parties' submissions*

147. As discussed at paragraph 140, the Parties submitted that they are not close competitors as competition takes place at the downstream level for PLD implementation software and that the choice of PCS software is secondary.

148. The Parties further submitted that Synopsys' closest competitors provide PLD implementation software which compete with OptoCompiler, including Cadence, Siemens, and Luceda.[215]

*CMA's assessment*

149. The Parties' internal documents show that they consider PLD implementation software to be important software used in the photonic chip design process (particularly Synopsys' documents), but that this does not stop competition from also taking place directly at the PCS level. Synopsys' documents from 2023 refer to Synopsys competing with Ansys' Lumerical for PCS, including one document referring directly to [✂] competing with Ansys' [✂] for [✂].[216] Similarly, Ansys' documents over the past couple of years refer to Ansys competing against Synopsys in PCS with OptSim listed as a competing product to Lumerical Interconnect.[217]

150. However, some Synopsys internal documents indicate that Synopsys focuses primarily on providing an integrated photonic design solution, whereas Ansys focuses on supplying Lumerical Interconnect as an input for third party PLD implementation software suppliers.[218] For example, Synopsys' internal documents indicate that Synopsys benefits from a '[✂]' due to offering a [✂] solution.[219] The CMA understands that while [✂] customers use Synopsys' OptSim with third-party PLD implementation software, Synopsys does not actively pursue [✂]-only opportunities.[220] The CMA notes in this respect that the revenue shares in Table 3 include all revenues generated by Synopsys from OptSim (ie including both from customers that purchase OptSim and OptoCompiler and from customers that purchase OptSim on a standalone basis for use with a third party PLD implementation software).

151. While a material proportion of third parties consider that the Parties compete closely for PCS software,[221] with one customer noting that the scope and functions

[215] FMN, paragraphs 14.213-14.215.
[216] Synopsys' Internal Document, Annex Q10(SNPS) – 043, '[✂]', 19 October 2023, page 36. Synopsys' Internal Document, Annex SNPSCMA-00001221, '[✂]', June 2023, page 15.
[217] Ansys' Internal Document, Annex Q9(ANSS) – 042, '[✂], April 2022, page 2.
[218] Synopsys' Internal Document, Annex Q9(SNPS) – 040, '[✂]', 30 August 2022, page 6; Ansys' Internal Document, Annex s.109(1)(ANSS)-1115, '[✂]', 13 October 2023, page 27.
[219] Synopsys' Internal Document, Annex Q9(SNPS) – 040, '[✂]', 30 August 2022, page 6.
[220] Parties' response to the CMA's RFI 9, paragraph 12.1. FMN, paragraph 14.214.
[221] Responses to the CMA's questionnaire from a number of third parties, October 2024.

of the Parties' products are almost equivalent,[222] the vast majority of respondents that considered that the Parties compete closely did not identify OptSim and Lumerical Interconnect as the relevant competing software and often referenced the Parties' broader portfolios in photonic software for photonic chips. The remaining third parties did not consider the Parties to be close competitors,[223] with two customers noting they were not aware of Synopsys' being active in PCS.[224]

152. When asked to list providers of PCS software and other types of software that can be used for photonic simulation,[225] Ansys' Lumerical Interconnect was mentioned most frequently. Consistent with the picture reflected in the shares of supply, the vast majority of customers rated Lumerical Interconnect as either very strong or strong.[226] In contrast, OptSim was mentioned considerably less frequently and rated as average/weak software.[227] One customer noted that it was 'buggy, and difficult to integrate'.[228]

153. The CMA considers that the evidence above indicates that the Parties have different offerings, namely Synopsys focuses on competing via its integrated photonic design flow (PCS + PLD implementation software) while Ansys competes with its PCS software for customers that use PLD implementation software supplied by Synopsys' rivals, in particular Cadence and Siemens. Further, the evidence shows that Ansys is the leading supplier of PCS software and that Lumerical Interconnect is strong, while Synopsys' OptSim is generally considered by third parties to be weaker and not a close alternative to Lumerical Interconnect.

*Alternative constraints*

*Parties' submissions*

154. The Parties submitted that there are numerous other suppliers of PCS software, including VPI Photonics, Optiwave Systems, Photon Design and Luceda, all of which are foundry certified.[229]

155. The Parties further submitted that not all customers use PCS software during their chip design process.[230] They submitted that PCS is a small, niche segment, with customer and foundry preferences shifting rapidly towards a new alternative option to conduct photonic chip simulation, namely using an electrical simulator (which does not require PCS software) in combination with pre-developed models in

[222] Response to the CMA's questionnaire from a third party, October 2024.
[223] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[224] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[225] The CMA asked customers to list all providers (including the ones that they currently use) of PCS software tools and/or other types of tools that can be used to meet their simulation requirements for photonic chips.
[226] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[227] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[228] Response to the CMA's questionnaire from a third party, October 2024.
[229] FMN, paragraph 14.218. Parties' additional response to the Issues Letter, 27 November 2024, paragraph 4.16.
[230] FMN, paragraph 14.123.

industry-standard Verilog-A language (the '**Verilog-A Option**').[231] Verilog-A models can be obtained from leading foundries, developed in-house, or sourced from vendors like Lumerical Interconnect.[232]

156. Synopsys submitted that it views foundries using the Verilog-A Option as an increasing [✂] to OptSim and sees [✂] as the preferred solution for customers and foundries, with foundries encouraging customers to use the Verilog-A Option.[233] Ansys estimates that around [✂]% of all of Lumerical Interconnect's customers that use Cadence's Spectre with Lumerical Interconnect use Verilog-A models.[234] The Parties submitted that Spectre (which is used with a Verilog-A model) is marketed for use in photonic chip design, and benchmarked against Synopsys' OptSim by foundries,[235] some of which (TSMC and GlobalFoundries) support the use of the Verilog-A Option.[236]

*CMA's assessment*

157. The CMA has assessed the extent to which (i) alternative suppliers of PCS software, and (ii) suppliers of the Verilog-A Option (ie, suppliers of electrical simulators that are used with Verilog-A models) would provide a competitive constraint on the Merged Entity post-Merger.

*Alternative PCS software*

158. The available evidence indicates that several alternative PCS software suppliers would remain available post-Merger, in particular VPI Photonics and Photon Design, as well as from new entrant Keysight, but that Luceda and Optiwave would pose relatively weak constraints.

159. Both Parties' internal documents refer to a broad range of rivals in this market and indicate that [✂], [✂], [✂] and [✂] compete for PCS software.[237] In addition, a Synopsys document indicates that it lost [✂] (an OptSim customer) to [✂].[238] The CMA understands that Keysight has recently entered the market for PCS software with its tool Photonic Designer.[239]

160. However, the evidence from third parties indicated that VPI Photonics and Photon Design are relatively stronger constraints than Luceda (who the CMA understands is primarily active through its integrated photonic design software IPKISS (similar

[231] Verilog-A is a behavioural modelling language common to all circuit simulators. The Parties submitted that an electrical simulator such as Spectre equipped with a photonic Verilog-A model can perform photonic chip simulation (FMN, footnote 258). Parties' additional response to the Issues Letter, 27 November 2024, paragraphs 4.5-4.6.
[232] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 4.11.
[233] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 4.12.
[234] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 4.10.
[235] Parties' response to the CMA's request for information, 13 August 2024 (RFI4), paragraph 3.3.
[236] Parties' submission to the CMA, 22 October 2024, paragraphs 2.4-2.5. FMN, paragraphs 14.219-220.
[237] Synopsys' Internal Document, Annex Q9(SNPS) - 043, '[✂]', 19 October 2023, page 36; Ansys' Internal Document, Annex s.109(1)(ANSS)-1009, '[✂]', 16 August 2023, page 7.
[238] Synopsys' Internal Document, SNPSCMA-00000724, '[✂]', 10 July 2022, page 9.
[239] Photonic Designer | Keysight.

to Synopsys) rather than a standalone PCS offering[240]) or Optiwave. When asked about PCS software alternatives and their relative strength, third parties rated alternatives to be of the same or greater strength than Synopsys' OptSim (rated weak/average). Photon Design was rated strong,[241] VPI Photonics was rated weak/average,[242] and one competitor told the CMA that it partners with VPI Photonics and Optiwave to offer PCS in response to customer demand.[243] However, Optiwave was rated weak[244] and Luceda was mentioned as an alternative by only one competitor and no customers.[245]

*The Verilog-A Option*

161. The CMA considers that there is some evidence to support the Parties' submission that the Verilog-A Option is increasingly an alternative option to using PCS software. Some of Synopsys' internal documents show Synopsys responding to the [✂] to [✂] from the use of Cadence's [✂] with [✂],[246] including plans to develop [✂] (Synopsys' [✂]) to allow it to compete via the [✂], which is being supported by foundries such as [✂] and [✂]. One document from October 2023 states, 'we need to establish [✂] as a [✂] solution, to avoid a [✂] vs [✂] (only) competitive situation' and notes that Cadence is the [✂] solution and drives foundries/customers to use [✂] and [✂].[247]

162. Synopsys' internal documents also suggest that it considers that there will be increasing uptake of [✂] in the future, and that Cadence will benefit from a pre-installed user base for its downstream PLD implementation software, as customers already use Cadence's software for electronic designs. The document states that this is Synopsys' '[✂]' to becoming a [✂] in the photonic chip market.[248] A Synopsys document from 2023 states that [✂] is adamant about using [✂] for photonic simulation.[249] The CMA did not see any evidence of the Verilog-A Option increasingly being an alternative option to using PCS software in Ansys' internal documents.

163. One customer also noted that Cadence's Spectre is a strong alternative for PCS software.[250] Another customer noted that it does not require specific PCS software as it designs a mix of electronic and photonic chips rather than pure photonic chips

[240] Response to the CMA's questionnaire from a third party, October 2024.
[241] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[242] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[243] Response to the CMA's questionnaire from a third party, October 2024.
[244] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[245] Response to the CMA's questionnaire from a third party, October 2024. No rating was provided by this third party.
[246] Annex RFI 25 Q 3.3 to the Parties' response to the [✂] Request for Information, 3 December 2024, October 2023, pages 5, 15, and 21. Annex RFI 25 Q 3.2 to the Parties' response to the [✂] Request for Information, 3 December 2024, February 2022, page 4. Annex RFI 25 Q 3.1 to the Parties' response to the [✂] Request for Information, 3 December 2024, November 2022, page 1.
[247] Annex RFI 25 Q 3.3 to the Parties' response to the [✂] Request for Information, 3 December 2024, October 2023, pages 5, 15, and 21.
[248] Synopsys' Internal Document, Annex Q9(SNPS) – 041, '[✂]', 1 September 2022, page 49.
[249] Synopsys' Internal Document, SNPSCMA-00001244, '[✂]', 16 July 2023, page 2.
[250] Response to the CMA's questionnaire from a third party, October 2024.

and can therefore use the photonics components modelised in Verilog-A Option with electrical simulators such as Cadence's Spectre.[251]

164. The CMA understands that Keysight's PathWave ADS and Siemens' AFS can also be used with Verilog-A models.[252] However, the CMA has not seen any evidence of this in either of the Parties' internal documents, and these alternatives were not mentioned by third parties responding to the CMA's questionnaire.

165. Although foundries' views as to the potential future prevalence of the Verilog-A Option as an alternative to current PCS software varied, the majority indicated that Verilog-A models with electrical simulators are an alternative to traditional PCS software.[253] In line with the Parties' submissions, one foundry stated that due to the installed-base of electrical simulators, uptake of the Verilog-A Option is likely to increase over the next five years.[254] Another foundry noted that it expects the use of the Verilog-A Option to increase as the complexity and scale of silicon photonics chips increases.[255]

*Conclusion on theory of harm 5*

166. For the reasons set out above, the CMA considers that the Parties do not compete closely in the supply of PCS software given that (i) Synopsys focuses on providing customers with an integrated PCS and PLD software (rather than standalone PCS software), whereas Ansys focuses on supplying Lumerical Interconnect to customers that use third party PLD implementation software which require PCS and (ii) Synopsys' OptSim is a comparatively much weaker solution that does not pose a strong constraint to Ansys' established product Lumerical Interconnect. While the Merger will strengthen Ansys' strong position in PCS software, there are several remaining PCS software suppliers, including Photon Design and VPI Photonics, as well as recent entrant Keysight. There is also evidence to indicate that additional constraints from suppliers of the Verilog-A Option, such as Cadence's Spectre, will provide a moderate but likely growing constraint on the Merged Entity.

167. Accordingly, the CMA found that the Merger does not give rise to a realistic prospect of an SLC as a result of horizontal unilateral effects in relation to the supply of PCS software globally.

[251] Response to the CMA's questionnaire from a third party, October 2024.
[252] Parties' response to the [✂] Request for Information, 3 December 2024, paragraphs 3.15 and 3.16.
[253] Third-party response to the CMA's Request for Information, 3 December 2024.
[254] Third-party response to the CMA's Request for Information, 3 December 2024.
[255] Third-party response to the CMA's Request for Information, 3 December 2024.

## Vertical effects

*Theory of Harm 6: Vertical effects in the supply of photonic layout design (PLD) implementation software for photonic chips globally*

168. Vertical mergers are those between firms active at different levels of the supply chain in the same industry (ie an upstream firm and a downstream firm), so competition in one market could be directly affected by outcomes in the other. A potential concern with vertical mergers is that they may result in the foreclosure of current or potential rivals – that the merged entity will be able to use its position in one market to harm the competitiveness of its rivals in the other. This would weaken the constraints that the merged entity faces and as a result harm competition and therefore customers. The concern with an input foreclosure theory of harm is that the merged entity may use its control of an important input to harm its downstream rivals' competitiveness, for example by refusing to supply the input (total foreclosure) or by increasing the price or worsening the quality of the input (partial foreclosure). This might then harm overall competition in the downstream market, to the detriment of customers.[256]

169. The CMA has assessed whether it is or may be the case that the Merger may be expected to result in an SLC as a result of input foreclosure in the supply of PLD implementation software globally. As discussed in paragraph 142, Synopsys and Ansys are both active upstream in the supply of PCS software, via OptSim and Lumerical Interconnect respectively. Synopsys (but not Ansys) is also active downstream in PLD implementation software via OptoCompiler.

170. The CMA has assessed whether the Merged Entity could use its market position in PCS software (where, as set out in Theory of Harm 5: Horizontal unilateral effects in the supply of PCS software tools for photonic chips globally, the CMA considers Ansys to have a strong position) to harm the competitive position of its rivals in the supply of PLD implementation software. There is not a conventional supplier/customer relationship between PCS software suppliers and PLD implementation software suppliers given PLD implementation software customers purchase PCS software directly from PCS software suppliers. However, as discussed further below, a PLD implementation software supplier's competitiveness is affected by whether its software interoperates with PCS software.[257]

171. Considering the above, the CMA has applied the framework set out in its merger guidelines for input foreclosure, assessing whether:[258]

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[256] CMA129, paragraphs 7.1(a), 7,2 and 7.9.
[257] As noted in CMA129, paragraph 7.11, the CMA may use its input foreclosure framework when assessing situations where a firm could use its position in one market to directly harm the competitiveness of its rivals by eg deteriorating interoperability.
[258] CMA129, paragraphs 7.10-7.11.

(a) the Merged Entity would have the ability to use its position in PCS software (primarily through Ansys' Lumerical Interconnect) to harm the competitiveness of its rivals for PLD implementation software;

(b) it would have the incentive to do so; and

(c) the foreclosure of these rivals would substantially lessen overall competition in PLD implementation software globally.

*Ability to foreclose rivals*

*Parties' submissions*

172. The Parties submitted in relation to:

(a) **the importance of PCS software for use with PLD implementation software**: that the choice of PCS software is secondary and does not significantly influence a customer's choice of PLD implementation software,[259] and not all customers require PCS software whereas PLD implementation software are essential.[260] Further, while Ansys' Lumerical Interconnect currently interoperates with Cadence's PLD implementation software (Virtuoso), interoperability with Lumerical Interconnect is not essential to Cadence's competitive strategy;[261] and

(b) **Ansys' market power in PCS software**: that the Merged Entity would not have market power in the supply of PCS software as there are several alternative options to Lumerical Interconnect including (i) alternative PCS software and (ii) the increasing use of the Verilog-A Option (detailed in paragraphs 155 to 156). In particular, Cadence provides an alternative to PCS software via the latter method.[262] In addition, customers can and do devise their own workarounds via interoperability scripts to stitch their desired PCS software and PLD implementation software together.[263]

*CMA's assessment*

173. To assess the Merged Entity's ability to foreclose, the CMA has considered:

(a) the importance of PCS software for use with PLD implementation software;

(b) whether the Merged Entity would have market power in PCS software and to what extent Synopsys' PLD implementation software competitors would be reliant on the Merged Entity; and

[259] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 6.13.
[260] FMN, paragraph 14.217. Parties' additional response to the Issues Letter, 27 November 2024, paragraphs 6.15.
[261] FMN, paragraph 14.217.
[262] Parties' additional response to the Issues Letter, 27 November 2024, paragraphs 6.4-6.6.
[263] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 6.12.

(c) the mechanisms that the Merged Entity could use to foreclose Synopsys' PLD implementation software rivals.

*Importance of PCS software for use with PLD implementation software*

174. The CMA considers that the evidence shows that PCS software is currently important to the overall photonic chip design process for some customers, and it is not necessary for the choice of PCS software to be more important than the choice of PLD implementation software for foreclosure concerns to exist. As set out in paragraph 143, the majority of customers said that they (i) require PCS software to design a photonic chip and (ii) consider/purchase PCS software alongside PLD implementation software.

175. Two competitors told the CMA that all PLD implementation software customers require PCS software.[264] One highlighted that this is due to the time and cost associated with photonic chip failure; simulation ensures that photonic chips work as intended the first time.[265]

*Merged Entity's market power in PCS software*

176. As set out in Theory of Harm 5: Horizontal unilateral effects in the supply of PCS software tools for photonic chips globally, the Merged Entity would have a strong market position in PCS software post-Merger, in particular through Ansys' market-leading product Lumerical Interconnect, which indicates that the Merged Entity would have a degree of market power in PCS software. Further, additional third-party feedback also indicates the importance of Lumerical Interconnect with respect to rivals' PLD implementation software. Two competitors stated that the majority of their PLD implementation software customers use Lumerical Interconnect, with one stating that Lumerical Interconnect features in virtually every design.[266]

177. However, the evidence also indicates that several credible alternative providers of PCS software are present in the market, with Siemens noting that it also partners with VPI Photonics, Optiwave and Luceda to offer PCS (as well as with Lumerical Interconnect) indicating other PCS software alternatives are credible.[267] Further, as noted in paragraph 166, the Merged Entity would face an increasing constraint from the Verilog-A Option (including through the combination of Cadence's Spectre and Siemens' AFS; both electrical simulation software that can be used in combination with a Verilog-A model). While several internal documents indicate that Synopsys considers Cadence to be [✂] Ansys' Lumerical Interconnect to

[264] Third-party response to the CMA's request for information, 10 September 2024, RFI1, paragraphs 4.1 and 6.1. Response to the CMA's questionnaire from a third party, October 2024.
[265] Third-party response to the CMA's request for information, 10 September 2024, RFI1, paragraphs 4.1 and 6.1.
[266] Third-party response to the CMA's request for information dated 10 September 2024, RFI1, paragraph 6.1. Response to the CMA's questionnaire from a third party, October 2024.
[267] Response to the CMA's questionnaire from a third party, October 2024.

compete in the market for PLD implementation software,[268] as discussed in paragraphs 161 and 162, there is also some evidence that indicates that Synopsys views Cadence's Spectre with a Verilog-A model as a [✂].

178. The evidence also indicates that customers can and do devise their own interoperability scripts to connect their PLD implementation software to their choice of PCS software – for example, the CMA understands that one customer uses Synopsys' OptSim alongside Cadence's Virtuoso and another uses OptSim alongside Luceda's IPKISS despite Synopsys never having developed any interoperability flows between OptSim and third-party suppliers of PLD implementation software.[269]

179. Based on the evidence above, the CMA considers that the Merged Entity would have a degree of market power in the supply of PCS software, in particular given the leading position of Lumerical Interconnect, and that Lumerical Interconnect is often used with rival PLD implementation software.

*The mechanisms the Merged Entity could use to foreclose Synopsys' PLD implementation software competitors*

180. The CMA considers that the Merged Entity could harm the competitiveness of Synopsys' PLD implementation software competitors by degrading/delaying (partial foreclosure) or removing (total foreclosure) the interoperability of its PCS software (in particular Lumerical Interconnect) with certain rival PLD implementation software. The CMA notes that, pre-Merger, Luceda offers a vertically integrated photonic design platform IPKISS, which incorporates both PLD implementation software and PCS software and does not partner with Ansys' Lumerical Interconnect and therefore could not be foreclosed.[270] The CMA therefore considers that the existing PLD implementation software suppliers that could be foreclosed are Cadence and Siemens.

181. Evidence from third parties indicates that the Merged Entity may be able to make Lumerical Interconnect technically inoperable with rival PLD implementation software. For example, some PLD implementation software customers and competitors expressed concerns regarding the interoperability of Lumerical Interconnect with Cadence's PLD implementation software post-Merger and said that they considered that it would be technically possible for the Merged Entity to restrict interoperability.[271]

[268] Synopsys Internal Document, Annex Q9(SNPS) – 041, '[✂]', 1 September 2022, page 32; Synopsys Internal Document, Annex Q9(SNPS) – 042, '[✂]', 25 January 2023, page 13.
[269] Parties' response to the CMA's RFI 9, paragraph 12.1. FMN, paragraph 14.214.
[270] Parties' response to the CMA's RFI 10, paragraphs 1.1 and 1.6.
[271] Response to the CMA's early invitation to comment. Response to the CMA's early invitation to comment. Submission to the CMA from a third party, April 2024, paragraphs 2.4 and 2.13.

*CMA's view on ability to foreclose*

182. The CMA considers that interoperability between PCS software and PLD implementation software is important for the competitiveness of rival PLD implementation software suppliers, that the Merged Entity would have a degree of market power in the supply of PCS software and that there are several mechanisms that the Merged Entity could use (namely through reducing the interoperability between PCS and PLD software) to harm the competitiveness of some of its PLD implementation software competitors that do not have their own integrated offering. Therefore, while the CMA recognises that there are credible alternatives to the Merged Entity in the supply of PCS software and that the Verilog-A Option also provides a likely increasing constraint, the CMA believes the Merged Entity would have some ability to foreclose competitors in the supply of PLD implementation software globally.

*Incentive to foreclose*

*Parties' submissions*

183. The Parties submitted, in relation to potential foreclosure of rival PLD implementation software competitors, that while Synopsys' OptoCompiler competes with Cadence's Virtuoso, there would be no incentive to degrade interoperability as:

(a) **reducing or terminating interoperability would result in financial loss:** given (i) revenue from Lumerical Interconnect depends on integration with a PLD implementation software to compete and (ii) the value of Lumerical Interconnect is associated with its ability to interoperate with a range of EDA tools;[272]

(b) **the Merged Entity would have no way of recouping the lost revenue:** additional sales of OptoCompiler would not be sufficient. Customers would switch to a different simulation tool to use with Cadence's Virtuoso[273] rather than switching to OptoCompiler, due to PLD implementation software driving customer choice;[274]

(c) **response of photonics customers:** customers would oppose any attempt from the Merged Entity to delay, degrade or remove interoperability between PCS and PLD implementation software;[275] and

(d) **a foreclosure attempt would be detectable and put Synopsys' wider EDA business at risk:** any delay, degradation or removal of interoperability

[272] Parties' additional response to the Issues Letter, 27 November 2024, paragraphs 6.19-6.20; FMN, paragraph 14.216.
[273] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 6.25 and Parties' response to RFI 4, paragraph 2.9.
[274] FMN, paragraph 14.216. The Parties also submitted the same reasons as for other interoperability concerns, specifically (1) interoperability is customer driven, and (2) Synopsys has a history of maintaining interoperability. Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraphs 6.18.
[275] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 6.2.

would put Synopsys' reputation and customer relationships at risk,[276] while the potential proportion of diverted sales away from Virtuoso for photonic chip design is likely to represent a tiny fraction of Virtuoso's revenues.[277]

*CMA's assessment*

184. To assess the Merged Entity's incentive to foreclose, the CMA has assessed:

(a) The closeness of competition between the Merged Entity and rivals that could be impacted by a foreclosure strategy; and

(b) Customer responses to attempted foreclosure.

*Closeness of competition*

185. The CMA has considered how closely Synopsys currently competes with rival PLD implementation software suppliers, as the gain in downstream sales would be greater if the Merged Entity had a strong downstream offering, and if it competed closely with the rivals that may be foreclosed.[278]

186. Table 4 sets out the CMA's estimated shares of supply of PLD implementation software by revenue in 2023.

**Table 4: PLD implementation software (by revenue, global, 2023)**

| **Supplier** | **Share** |
|---|---|
| Synopsys | 20-30% |
| Luceda | 30-40% |
| Cadence | 20-30% |
| Siemens | 5-10% |
| Latitude | 0-5% |
| **Total** | **100%** |

Source: CMA analysis based on the Parties and competitor data[279]

187. Table 4 shows that Luceda, Cadence and Synopsys have the largest market positions, although the CMA considers Luceda's share is likely to be overstated.[280] Siemens (5-10)% and Latitude (0-5)% have notably smaller shares.

[276] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 6.19.
[277] Parties' additional response to the Issues Letter, 27 November 2024, paragraph 6.25
[278] CMA129, paragraph 7.19b.
[279] FMN, Table 19. Responses to the CMA's questionnaire from a number of third parties, October 2024. The CMA did not receive third party evidence from one competitor and has supplemented the data with the Parties' estimates.
[280] The CMA notes that Luceda's share is likely to be slightly overstated.

188. Over 2022 and 2023, Synopsys' internal documents refer to Cadence as its [✂] competitor and the [✂] to Synopsys becoming the [✂].[281] Feedback from customers also indicates that Synopsys and Cadence compete particularly closely, with both suppliers identified by third parties as having the strongest PLD implementation software,[282] followed by Siemens and then Luceda, which customers considered comparatively weaker.[283]

189. The CMA therefore considers that the Merged Entity would be in a position to achieve some downstream gains in PLD implementation software, given its strong market position, but that Luceda would also be likely to gain some downstream customers in the event of foreclosure, given it offers a vertically integrated product and competes effectively pre-Merger without a partnership with Lumerical Interconnect.[284]

*Customer response to attempted foreclosure*

190. The CMA considers that the Merged Entity's incentive to reduce or terminate interoperability of Lumerical Interconnect with competitors' PLD implementation software depends on how customers would alter their PCS and PLD implementation software purchasing habits in response to foreclosure attempts by the Merged Entity. If customers are more likely to switch PLD implementation software supplier than PCS software supplier then the Merged Entity would have greater incentive to foreclose PLD implementation tool rivals.

191. When customers were asked what they would do if Lumerical Interconnect no longer interoperated with their PLD implementation software, responses were mixed. Around half of customers stated they would switch PLD implementation software, with one customer stating that they would use software that worked with Lumerical Interconnect.[285] Another customer said that it would likely switch to Synopsys' combined photonic solution (that is, the combination of OptSim and OptoCompiler), as the simulation and implementation software need to work together as a whole.[286] However, the other half of customers said they would switch PCS software with one customer noting they could switch to Photon Design's PICWave,[287] and another customer noting that in the long term it would seek alternatives to Lumerical Interconnect that ensured full freedom on interoperability across software,[288] which would result in upstream losses and no downstream gains for the Merged Entity.

192. Further, a Synopsys internal document from May 2024 notes that Synopsys was [✂] in getting a customer to switch to OptSim as its PCS software and the

[281] Synopsys' Internal Document, Annex Q9(SNPS) – 042, '[✂]', 25 January 2023, page 13; Synopsys' Internal Document, Annex Q9(SNPS) – 041, '[✂]', 1 September 2022, page 49.
[282] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[283] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[284] Parties' response to the Issues Letter, 27 November 2024, paragraph 6.6.
[285] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[286] Responses to the CMA's questionnaire from a number of third parties, October 2024.
[287] Response to the CMA's questionnaire from a third party, October 2024.
[288] Response to the CMA's questionnaire from a third party, October 2024.

customer could not see itself running [✂] ([✂] or [✂]) outside of [✂] environment,[289] and that it was working with foundries ([✂] and [✂]) that create photonic models using [✂].[290] This suggests that the choice of PLD implementation software is important to customers and that there are alternative options to PCS software.

193. Based on the evidence above, the CMA considers that in the event that the Merged Entity pursued a foreclosure strategy, customers would be as likely to switch PCS software provider as to switch PLD implementation software provider.

*CMA's view on incentive*

194. On the basis of the evidence above, the CMA considers that, on balance, the Merged Entity would not have the incentive to foreclose PLD implementation software rivals. Evidence suggests customers would be equally likely to switch PCS software supplier if Lumerical Interconnect no longer interoperated with their PLD implementation software they would be to switch PLD implementation software provider. Of those that would switch PLD implementation software provider, some would likely switch to Luceda (which does not rely on Lumerical Interconnect). Finally, some PLD implementation software customers do not use PCS software and therefore PLD implementation software rivals supplying these customers would not be at risk of losing them following foreclosure.

*Conclusion on theory of harm 6*

195. For the reasons set out above, the CMA believes that while the Merged Entity would have some ability to foreclose PLD implementation software rivals, the weight of the evidence indicates that it would, overall, not have the incentive to do so. Given the CMA believes that the Merged Entity would have no incentive to foreclose it has not considered the effect of foreclosure.

196. Accordingly, the CMA found that the Merger does not give rise to a realistic prospect of an SLC as a result of input foreclosure in the supply of PLD implementation software globally.

**Conglomerate effects**

*Theory of Harm 7: Conglomerate effects resulting in the foreclosure of Synopsys competitors by leveraging Ansys' position*

197. The Parties have, broadly speaking, differing strengths in the chip design flow, with Synopsys primarily active in EDA and Ansys primarily active in S&A (see paragraphs 16 and 17 for a description of the Parties' activities).

[289] The CMA has interpreted this reference to Virtuoso as covering the Virtuoso environment, which includes Spectre.
[290] Annex RFI 25 Q 3.4 to the Parties' response to the [✂] Request for Information, 3 December 2024, page 1, May 2024.

198. As noted previously, customers designing chips require both EDA and S&A software, and, increasingly, S&A software is used by the customer earlier in the design flow alongside EDA software (see paragraph 20). The CMA notes that the rationale for the Merger is to allow Synopsys to develop 'comprehensive and seamless design solutions through deeper technical integration' that combines Synopsys' and Ansys' capabilities.[291]

199. Given the above, the CMA has considered whether the Merger may result in the foreclosure of current or potential rivals through conglomerate effects, by allowing the Merged Entity to use its position in one market to harm the competitiveness of its rivals in another market.[292] Specifically, the CMA has assessed whether the Merged Entity may restrict its rivals in 'focal markets' from competing for customers by using its strong position in 'adjacent markets.'[293] The CMA has focussed its assessment on the following focal and adjacent markets in which some third parties have raised concerns:

(a) In relation to focal markets, the CMA has focussed on the impact of the Merger on rivals' competitiveness in the global supply of: place and route software in each of digital, analog, mixed and multi-die chips; circuit simulation software in each of analog, mixed and multi-die chips; parasitic analysis software in each of digital, analog, mixed and multi-die chips; and timing analysis software in each of digital, analog, mixed and multi-die chips ('**the focal markets'**).

(b) In relation to adjacent markets, the CMA has considered the strength of Ansys' position in the following areas: the global supply of gate-level power integrity analysis for digital and multi-die chips (both considered in **Theory of Harm 7a**); thermal analysis for multi-die chips (considered in **Theory of Harm 7b**); transistor level power integrity analysis for analog chips (considered in **Theory of Harm 7c**); and electromagnetic simulation analysis for both analog and multi-die chips (both considered together in **Theory of Harm 7d**) ('**the adjacent markets**').[294]

200. A very small minority of third parties raised concerns relating to the ability of the Merged Entity to encourage customers to purchase Synopsys' EDA software by leveraging the strength of certain Ansys' S&A software, by delaying, degrading, or removing interoperability of Ansys' software with third party EDA software, and/or by bundling Synopsys' and Ansys' software together.[295] In particular, several third parties identified the 'RedHawk software (RedHawk/RedHawk-SC and RedHawk-SC ET), as well as HFSS and Totem, as software that provide Ansys with a strong

[291] FMN, paragraph 12.
[292] CMA129, paragraph 7.2.
[293] CMA129, paragraph 7.30.
[294] The CMA has focused on analog, digital and multi-die chip design flows and received limited feedback in relation to mixed signal chip design flows. Where the relevant product is applicable for use in multiple types of chip designs, the CMA has combined its assessment of the impact on those markets as the competitive assessment did not materially differ as between the different chip designs.
[295] Responses to the CMA's questionnaire from a number of third parties, October 2024.

position in the adjacent markets identified above. These third parties submitted that such actions could foreclose rivals and lead to less choice for customers.

201. The Parties submitted that there is no realistic scenario in which there would be an SLC through Synopsys utilising Ansys' products to foreclose rivals (noting that, in particular, Synopsys' EDA software need to be interoperable with third party software in order to function, and it is essential to offer this interoperability in order to compete).[296] Further detail relating to submissions from the Parties are included below (in relation to the Merged Entity's ability and incentive to foreclose rivals post-Merger, where appropriate).

202. The CMA has used the ability, incentive and effect framework to analyse this theory of harm.

*Ability to foreclose EDA competitors*

203. The CMA has considered the following factors to assess the ability to foreclose:

(a) Whether the Merged Entity would have market power in the supply of:

(i) gate-level power integrity analysis software in digital and multi-die chip flows globally;

(ii) thermal analysis software in multi-die chip flows globally;

(iii) transistor-level power integrity analysis software in analog chip flows globally;

(iv) electromagnetic simulation software in analog and multi-die chip flows globally;

(b) Whether it is feasible for the Merged Entity to offer customers a combined offer, either through having the technical ability to delay, degrade or remove interoperability with third party software whilst integrating its own software, or through bundling strategies.

204. The CMA has considered the extent of potential losses of sales by rivals as part of the assessment of the incentive to foreclose.

*Parties' submissions on ability*

205. The Parties submitted that they would not have the ability to foreclose rivals as the Merged Entity will be constrained by rivals (ie competitors can create or offer their own integrated solutions or bundles).[297] Further, Ansys' software in the adjacent markets are signoff software and simply act as a 'check' at the end of the design process and thus have no ability to influence customer choices in focal markets.[298] In addition, the Parties submitted that they have no means to harm rivals through

[296] FMN, paragraphs 19.1-19.2.
[297] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 7.10.
[298] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraphs 7.18 and 7.23.

bundling or tying.[299] Further submissions from the Parties relating to the RedHawk software and interoperability note that customers of the RedHawk software have strong alternatives, notably Cadence's Voltus, and these customers demand the ability to mix and match software and would reject any combined offers.[300] In relation to interoperability, the Parties stated that interoperability with third party software is necessary for the commercial viability of any software offering.[301]

*CMA's assessment*

*Theory of Harm 7a: The Merged Entity's competitive position in gate-level power integrity analysis for each of digital and multi-die chips*

206. Gate-level power integrity analysis software are an important part of the sign-off stage of the chip design flow. Power integrity software verify the power distribution of a chip design to ensure that there are no issues with voltage drop or other factors that could affect the reliability of the design. The key Ansys software in this space for digital and multi-die chips are RedHawk and RedHawk-SC. RedHawk-SC is a version of RedHawk offered on Ansys' SeaScape platform (a platform that allows for scalability and big data analytics).[302]

207. The evidence indicates that Ansys has a strong market position in these markets. The CMA estimated, based on data from the Parties and third parties, that Ansys has a share of [70-80]% globally by revenue in 2023, followed by Cadence with [20-30]% and Siemens with [0-5]%.[303]

208. The Parties' internal documents also attest to the leading market position of RedHawk and RedHawk-SC. As noted above in the context of the Merger rationale, Synopsys considers RedHawk and RedHawk-SC to be key. One Ansys internal document refers to RedHawk-SC as a '[✂] golden signoff [software]'[304] and another Ansys internal document states that RedHawk-SC is 'by far the [✂] [software] for chip signoff.'[305] One Synopsys document comparing competitors across different types of analysis notes RedHawk-SC has the [✂] position and [✂] with customers, with only Voltus also seen as a [✂] player in gate-level power integrity analysis.[306]

209. Similarly, the feedback from third parties also indicates that Ansys is the market leader. RedHawk and RedHawk-SC have been described by third parties as

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[299] FMN, paragraph 19.9.
[300] Synopsys' submission on why Synopsys could not leverage RedHawk to harm competitors, 5 September 2024, paragraph 4.
[301] Synopsys' submission on interoperability, 8 November 2024, paragraph 1.2.
[302] See https://www.ansys.com/products/semiconductors and https://www.solidbasetech.com/ansys/redhawk_sc#:~:text=RedHawk%2C%20the%20industry%20gold%2Dstandard,big%20data%20analytics%20of%20SeaScape.
[303] The same limitations identified in Theory of Harm 1 in relation to share of supply data apply, as do specific data limitations with third party data provided in relation to this overlap. Nevertheless, the CMA notes the very high shares of Ansys.
[304] Ansys' internal document, Annex Q9(ANSS) – 045, '[✂]', January 2024, page 12.
[305] Ansys' internal document, Annex s.109(1)(ANSS)-1820, '[✂]', 15 August 2022, page 1.
[306] Synopsys' internal document, Annex Q9(SNPS) – 065, '[✂]', 27 February 2023, slide 17.

'testament for Ansys being at the forefront of innovation,'[307] and a 'global leader' in gate-level power integrity (and electrothermal) analysis.[308]

210. The evidence indicates that the Merged Entity would face a significant competitive constraint in gate-level power integrity analysis from Cadence, while Siemens' software appear to exert a more limited constraint:

(a) Cadence offers a gate-level power integrity analysis software called Voltus, both on a standalone basis and as part of its integrated place and route software Innovus. Cadence also offers a number of other software that may share functionalities with RedHawk and RedHawk-SC (Joules and PVC PERC).[309] A large number of customers identified Voltus as an alternative to RedHawk/RedHawk-SC, and the majority of these customers identified it as a strong or very strong alternative.[310] The Parties provided evidence of a number of customers switching from RedHawk or RedHawk-SC to Voltus.[311] In addition, a small number of customers also considered each of Cadence's Voltus Fi, Joules and PVS PERC to be alternatives to Ansys' RedHawk and RedHawk-SC, although to a lesser extent than Voltus.[312] However, whilst customers identified Voltus as an alternative, the Parties' internal documents indicate that Cadence's software are comparatively [✂] than Ansys' RedHawk and RedHawk-SC: while Ansys benchmarks Cadence as a competitor in gate-level power integrity analysis,[313] one document notes that it considers Voltus a '[✂]'.[314] [315]

(b) Siemens offers a gate-level power integrity analysis software for digital and multi-die chips called mPower, as well as Calibre PERC, both of which it offers on a standalone basis.[316] mPower and Calibre PERC are foundry-certified (for a description of foundry certification, see the Industry overview section).[317] Siemens is rarely mentioned in Ansys' internal documents in relation to gate-level power integrity analysis for digital and multi-die chips. A number of third parties considered that Siemens' mPower or Calibre PERC

[307] Submission to the CMA from a third party, June 2024.
[308] Submission to the CMA from a third party, April 2024.
[309] Joules measures and reduces power consumption (https://www.cadence.com/en_US/home/tools/digital-design-and-signoff/power-analysis/joules-rtl-power-solution.html) and PVC PERC is a physical verification system https://www.cadence.com/en_US/home/resources/datasheets/cadence-physical-verification-system-ds.html).
[310] Response to the CMA's questionnaire from third parties, November 2024.
[311] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 7.12.
[312] Response to the CMA's questionnaire from third parties, November 2024.
[313] Ansys' internal document, Annex s.109(1)(ANSS) -1823, '[✂]', 6 September 2022, page 1. Ansys' internal document, Annex Q10(ANSS) -045, '[✂]', page 12.
[314] Ansys' internal document, Annex s.109(1)(ANSS)-1823, '[✂]', 6 September 2022, page 1.
[315] An internal document from Synopsys indicates that it may view Voltus to be weaker than RedHawk - when considering the potential outcomes of an acquisition by Cadence of Ansys, Synopsys implies that a divestment of Voltus would be less preferable than that of RedHawk, suggesting that it views Voltus as a weaker software product relative to RedHawk. Synopsys' internal document, Annex Q9(SNPS) – 009 – '[✂]', 27 November 2023, paragraph 5aii.
[316] Calibre PERC is a software product for reliability verification solutions (https://eda.sw.siemens.com/en-US/ic/calibre-design/reliability-verification/perc/).
[317] See: https://newsroom.sw.siemens.com/en-US/mpower-tower-ic-design/ and FMN, para 14.141.

was an alternative to Ansys' RedHawk and RedHawk-SC, although to a lesser extent than Voltus.[318]

(c) The CMA has not seen any further evidence from third-parties or internal documents to suggest that Ansys' gate-level power integrity analysis software face competitive constraints from any other providers in this market.

211. In relation to the relative ease or difficulty of switching from Ansys' product, around half of customers responding to the CMA's investigation reported that it would be either very difficult or difficult to switch from RedHawk/RedHawk-SC.[319] In particular, they noted that the process of moving to a different sign-off software is resource intensive and requires significant work.[320] Customers also indicated that switching would be expensive.[321] One customer suggested that it could take up to five years or more of engineering work to switch away from Ansys' RedHawk/RedHawk-SC. [322]

212. Accordingly, the CMA considers that RedHawk and RedHawk-SC have an important position in the global supply of gate-level power integrity analysis for digital and multi-die chips.

*Theory of harm 7b: The Merged Entity's competitive position in thermal analysis for multi-die chips globally*[323]

213. Thermal analysis software is an important part of the sign-off stage for multi-die chips. Thermal analysis software ensure that multi-die chips allow heat to dissipate. This is particularly important given the heat that occurs due to the stacking of multiple components in multi-die chips, which needs to be simulated to ensure the performance of the chip design. The key Ansys software in this space for multi-die chips is RedHawk-SC ET. RedHawk-SC ET also uses the SeaScape platform.[324]

214. The Parties' internal documents note the [✂] market position of RedHawk-SC ET. One internal document from Ansys indicates that RedHawk-SC ET is 'the only comprehensive chip-centric solution for power [and] thermal integrity analysis of 3DIC designs.'[325] Another Ansys' internal document considers that RedHawk-SC ET is a 'competitive' software for thermal analysis which consists of 'Ansys golden FEM solver'.[326]

215. As noted above, feedback from third parties also indicates that the Redhawk software (including RedHawk-SC ET) are clear market leaders. A summary of

[318] Response to the CMA's questionnaire from third parties, November 2024.
[319] Response to the CMA's questionnaire from third parties, November 2024.
[320] Response to the CMA's questionnaire from third parties, November 2024.
[321] Response to the CMA's questionnaire from third parties, November 2024.
[322] Response to the CMA's questionnaire from a third party, November 2024.
[323] The CMA's analysis in this market focused on the position and combination with multi-die chips specifically given that RedHawk-SC ET is focussed on electrical, thermal and mechanical sign-off of multi-die chips only.
[324] https://www.ansys.com/products/semiconductors/ansys-redhawk-sc-electrothermal.
[325] Ansys' internal document, Annex s.109(1)(ANSS)-1051, '[✂]', 8 September 2023, slide 40.
[326] Ansys' internal document, Annex s.109(1)(ANSS)-0791, '[✂]', 21 October 2023, slide 11.

third-party views relating to the importance of the RedHawk software is described at paragraph 209 in the section above. The CMA's share of supply estimates also indicate that the market is very concentrated and Ansys, along with Cadence and Siemens, are the only three suppliers with a material presence.[327]

216. The evidence indicates that the Merged Entity will face a significant constraint in thermal analysis from Cadence, and a relatively weak constraint from Siemens:

(a) Cadence offers a thermal analysis software called Celsius, and other software (Sigrity and Clarity) which the CMA understands can be used, although this is not typical, to conduct thermal analysis in multi-die chip flows.[328] Celsius, Sigrity and Clarity are available on a standalone basis[329] and are all foundry-certified.[330] These software are also offered as part of Cadence's integrated solution Integrity 3D-IC which is its place and route software for 3D IC chips. Cadence was the only provider which was identified as offering a strong or very strong alternative to Ansys' thermal analysis software RedHawk-SC ET by customers.[331] Several internal documents from Ansys benchmark Cadence against RedHawk-SC ET for thermal analysis in multi-die chips.[332] For example, in one internal document Ansys considers that RedHawk-SC ET competes with Cadence's Celsius. This document rates each competing software as either 'competitive,' 'available,' or 'lacking'- it considers RedHawk-SC ET to be '[✂]', and refers to Cadence's thermal analysis offerings as '[✂].'[333]

(b) Siemens offers a thermal analysis software called Flotherm on a standalone basis. Flotherm is foundry-certified.[334] In response to third-party questionnaires, only a very small number of customers identified Siemens Flotherm as an alternative and these customers indicated that Siemens' Flotherm is either an average alternative or a poor alternative to RedHawk-SC ET.[335] A few internal documents from Ansys show that it benchmarks RedHawk-SC ET against Siemens for thermal analysis in multi-die chips.[336] For example, in one internal document Ansys considers that RedHawk-SC ET competes with Siemens' Flotherm. However, the internal document describes Flotherm as '[✂].'[337]

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[327] As described above, the CMA has not placed weight on the specific share of supply estimates based on revenue from Ansys and third parties, due to significant limitations with the data. Moreover, other evidence collected indicated that the shares significantly understated Ansys' position.
[328] Response to the CMA's questionnaire from a third party, November 2024. And also see for example, Synopsys' internal document, SNPSCMA-00011245, '[✂]', March 2023, slide17.
[329] Submission to the CMA from a third party, April 2024.
[330] See: Cadence and Intel Foundry Collaborate to Enable Heterogeneous Integration with EMIB Packaging Technology | Cadence.
[331] Response to the CMA's questionnaire from a third party, November 2024.
[332] Ansys' internal document, Annex s.109(1)(ANSS)-0791, '[✂]', 21 October 2024, slide 11. Ansys' internal document, Annex s.109(1)(ANSS)-2210, '[✂]', 25 July 2024, slide 36.
[333] Ansys' internal document, Annex s.109(1)(ANSS)-0791, '[✂]', 21 October 2022, slide 11.
[334] See: Siemens partners with TSMC for 3nm product certifications an | Siemens Software.
[335] Response to the CMA's questionnaire from a number of third parties, November 2024.
[336] For example, Ansys' internal document Annex s.109(1)(ANSS)-0791, '[✂]', 21 October 2022, slide 11.
[337] Ansys' internal document, Annex s.109(1)(ANSS)-0791, '[✂]', 21 October 2022, slide 11.

(c) The CMA has not seen any further evidence from third-parties or internal documents to suggest that Ansys' thermal analysis software faces competitive constraints from other providers in this market.

217. In relation to the relative ease or difficulty of switching from Ansys' product, around a third of customers responding to the CMA's investigation reported that it would very difficult or difficult to switch from RedHawk-SC ET.[338] Half of the customers indicating that switching would be difficult or very difficult did so because of the lack of good alternatives,[339] whilst one customer noted the complexity of switching due to project specific requirements.[340]

218. Accordingly, the CMA considers that RedHawk-SC ET has an important position in the global supply of thermal analysis for multi-die chips.

*Theory of Harm 7c: The Merged Entity's competitive position in transistor- level power integrity analysis for analog chips globally*

219. As described at paragraph 96 in Theory of Harm 2, Ansys offers Totem which is a transistor-level power integrity analysis software for analog chip designs.

220. As discussed in Theory of Harm 2:

(a) Ansys' Totem has a strong market position with Cadence being the next largest competitor and all other competitors having notably smaller market positions.

(b) Third parties mentioned Ansys' Totem most frequently when asked about transistor-level power integrity analysis software that meet their requirements and consistently referred to it as the long-established industry-leading software.

(c) Totem faces a strong constraint from Cadence, alongside several smaller existing and expanding competitors.

221. In relation to the relative ease or difficulty of switching from Ansys' product, the CMA considers that similar considerations described above in relation to switching from Ansys' gate-level power integrity products are likely to be relevant to customers, and as such the costs to customers of switching are expected to be high.

222. Given the evidence above, the CMA considers that Totem has an important position in the supply of transistor-level power integrity analysis for analog chips globally.

[338] Response to the CMA's questionnaire from third parties, November 2024.
[339] Response to the CMA's questionnaire from a third party, November 2024.
[340] Response to the CMA's questionnaire from a third party, November 2024.

*Theory of Harm 7d: The Merged Entity's competitive position in electromagnetic simulation for analog and multi-die chips flows globally*

223. Electromagnetic simulation software is an important part of the sign-off stage. Electromagnetic simulation software verifies how a chip will respond to electromagnetic signals, in particular, to ensure that the chip will operate as intended and not be susceptible to, or create, electromagnetic interference. The key Ansys software in this space for both analog and multi-die chips is HFSS.[341]

224. The CMA estimates, based on revenues from Ansys and third parties, that Ansys has the largest share of supply of [40-50]% based on revenue globally in 2023 in the supply of electromagnetic simulation software, followed by Dassault [20-30]%, Siemens [10-20]% and Cadence [10-20]%. Keysight and Lorentz each have very low shares of [0-5]%.[342]

225. The Parties' internal documents note the leading market position of HFSS and indicate that HFSS is an important and strong software. For example, in one internal document Ansys indicates that HFSS is 'accepted as the industry [✂] for accuracy.'[343] Synopsys' internal documents also indicate that Ansys is a [✂] provider in the market for electromagnetic simulation. For example, in one internal document Synopsys refers to Ansys as the '[✂]' in this market,[344] and in another that Ansys' software is considered '[✂] (particularly [✂])'.[345]

226. Similarly, the feedback from third parties also indicates that HFSS is the clear market leader. HFSS has been described by third parties as 'the leading' electromagnetic product[346] and a 'critical' software that has a 'dominant' position.[347]

227. The evidence indicates that the Merged Entity would face a significant competitive constraint in electromagnetic simulation from Cadence and a material competitive constraint from Dassault:

    (a) Cadence offers an electromagnetic simulation software, Clarity, on a standalone basis and on an integrated basis as part of Cadence's Integrity 3D-IC which is its 3DIC place and route software. As noted above, Clarity is foundry-certified. A relatively large number of customers identified Clarity as an alternative to HFSS and nearly half of these customers rated it a strong or

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[341] See https://www.ansys.com/products/electronics/ansys-hfss?utm_campaign=product&utm_medium=paid-search&utm_source=google&utm_content=digital_electronics_copr15el_contact_contact-us_hfss-electronics-brand-search_1a_en_global&campaignid=7013g000000cXBXAA2&utm_term=ansys%20hfss&gad_source=1&gclid=EAIaIQobChMIk7jspNDtiQMVLqJQBh2jvh50EAAYASAAEgKcvPD_BwE. The CMA understands that Ansys also offers RaptorH as an electromagnetic simulation analysis software. However, this is not the focus of Theory of Harm 7 or Theory of Harm 9 given third-party feedback which indicates that HFSS is the main electromagnetic software offered by Ansys.
[342] As noted above, the same limitations identified in Theory of Harm 1 apply, as do specific data limitations with third party estimates in this overlap. Nevertheless, the CMA notes the very high shares of Ansys.
[343] Ansys' internal document, Annex s.109(1)(ANSS)-0772, '[✂]', 16 September 2024, slide 18.
[344] Synopsys' internal document, Annex Q9(SNPS) – 035, '[✂]', 1 January 2023, slide 3.
[345] Synopsys' internal document, Annex Q9(SNPS) – 065, '[✂]', 27 February 2023, slide 16; another Synopsys' document references Ansys HFSS as having '[✂]' (see Synopsys' internal document, Annex Q9(SNPS) - 038 – '[✂]', 1 August 2023, slide 65).
[346] Submission to the CMA from a third party, June 2024.
[347] Response to the CMA's questionnaire from a third party, October 2024.

very strong alternative to HFSS. [348] To a lesser extent, a small number of customers also considered Cadence's Sigrity, EMX and Celsius as alternatives to Ansys' HFSS.[349] The CMA has seen a limited number of Ansys' documents that mention Clarity, however, none of these documents clearly benchmark Clarity against HFSS.[350] In one internal document, Synopsys considers Cadence's Clarity a [✂] challenger to Ansys' HFSS. [351]

(b) A number of customers identified Dassault's CST as an alternative to HFSS and around half of these customers considered it to be a strong or very strong alternative to HFSS. In one internal document, Ansys benchmarks Dassault as one of its '[✂]' competitors globally and considers Dassault's CST as [✂] to Ansys' HFSS.[352]

228. There is some evidence to indicate that there is a tail of smaller competitors in electromagnetic simulation, including Siemens, that will exert a more limited constraint on the Merged Entity post-Merger:

(a) Siemens offers an electromagnetic simulation software called Hyperlynx on a standalone basis. Only a very small number of customers responding to the CMA's investigation identified it as an alternative to Ansys' HFSS.[353] However, in one internal document, Synopsys considers Siemens' Hyperlynx a [✂] challenger to Ansys' HFSS.[354]

(b) A limited number of customers also identified a long tail of other suppliers that offer software that can be used as alternatives to HFSS (for example, Keysight and Altair).[355] In one internal document, Ansys benchmarks Altair's Feko as offering a [✂] alternative to Ansys' HFSS.[356] The CMA has not seen any further evidence from third parties or internal documents to suggest that Ansys' HFSS faces strong competitive constraints from any of these other providers.

229. In relation to the relative ease or difficulty in switching away from Ansys' HFSS software, over half of customers responding to the CMA's investigation reported that it would be very difficult or difficult to switch away from HFSS. [357] In particular, customers indicated that the process of moving to a different electromagnetic simulation software would be expensive and resource intensive. [358] Around a third of customers that stated it would be difficult or very difficult to switch said this is because Ansys' HFSS is a 'gold standard solver' with few alternatives and that it is 'entrenched' in their chip design flows, with their design processes built around

[348] Response to the CMA's questionnaire from a number of third parties, November 2024.
[349] Response to the CMA's questionnaire from a number of third parties, November 2024.
[350] See Ansys' internal document, Annex s.109(1)(ANSS)-0791, '[✂]', 21 October 2022, slide 11.
[351] Synopsys' internal document, Annex SNPSCMA-00011245, '[✂]', 1 March 2023, slide 17.
[352] Ansys' internal document, Annex s.109(1)(ANSS)-1734, '[✂]', 29 March 2023, pages 3-4.
[353] Responses to the CMA's questionnaire from a third party, November 2024.
[354] Synopsys' internal document, SNPSCMA-00011245, March 2023, slide 17.
[355] Response to the CMA's questionnaire from a number of third parties, November 2024
[356] Ansys' internal document Annex s.109(1)(ANSS)-1734, pages 3-4.
[357] Response to the CMA's questionnaire from a number of third parties, November 2024.
[358] Response to the CMA's questionnaire from a number of third parties, November 2024.

HFSS.[359] A few customers considered that it would take years before they could switch to an alternative to Ansys' HFSS with one customer suggesting it would take up to three years to switch to a different software. [360]

230. Accordingly, the CMA considers that HFSS has an important position in the supply of electromagnetic simulation for analog and multi-die chips globally.

*Feasibility of combined offering and loss of sales by rivals*

231. The CMA has assessed whether it is feasible for the Merged Entity to offer customers a combined offer across the focal and adjacent markets described above, either through having the technical ability to delay, degrade or remove interoperability with third party software, or through bundling strategies. The CMA has also considered (see from paragraph 244 onwards) the extent to which this combined offer could deprive rivals of sales.[361]

232. The Parties submitted that they would not have the ability to offer software that did not interoperate effectively with third party software or force customers to purchase Synopsys' EDA software alongside Ansys' S&A software. In relation to the feasibility of a combined offer, the Parties submitted that: customers of RedHawk and other Ansys software have strong alternatives (notably Voltus),[362] customers demand the ability to mix and match software and such combined offers would be rejected by customers,[363] and interoperability with third party software is necessary for the commercial viability of any software offering.[364] The Parties also noted that strength in one market (for example, place and route) does not necessarily translate into strength in another, related, market (for example, timing analysis).[365]

*Evidence relating to the ability of the Merged Entity to offer a combined offering*

233. The CMA considered which combinations of focal and adjacent products could be attractive to customers. The CMA understands that all of Ansys' software in the adjacent markets (RedHawk and RedHawk-SC, Totem, RedHawk-SC ET and HFSS) need to work closely with place and route software and circuit simulation software (for example to ensure that circuit layouts designed using place and route software do not suffer from issues such as electromagnetic interference or overheating).[366] The CMA has also received feedback that parasitic analysis and

[359] Response to the CMA's questionnaire from a number of third parties, November 2024.
[360] Response to the CMA's questionnaire from a third party, November 2024.
[361] CMA129, paragraph 7.33.
[362] Synopsys' submission on why Synopsys could not leverage RedHawk to harm competitors, 5 September 2024, paragraph 4.
[363] Synopsys' submission on why Synopsys could not leverage RedHawk to harm competitors, 5 September 2024, paragraph 12.
[364] Synopsys' submission on interoperability, 8 November 2024, paragraph 1.2.
[365] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 7.22 onwards.
[366] Submission to the CMA from a third party, July 2024 and response to the CMA's questionnaire from a number of third parties, October 2024.

timing analysis software also need to work closely with Ansys' software in the adjacent markets.[367]

234. The CMA has considered the following evidence in relation to the ability of the Merged Entity to offer a combined offering of the software described in paragraph 233:

(a) The factors that are important to customers when purchasing EDA and S&A software, including the extent to which a bundled, discounted offer of EDA and S&A software would be attractive to customers; and

(b) The extent to which the Parties could delay, degrade or remove interoperability between their software and those of third parties.

235. As noted in the Background and nature of competition section, customer evidence shows that customers overwhelmingly see the quality and technical capabilities of a software as a very important factor when purchasing products. The need for software to be interoperable with third party software is another important or very important factor for over three-quarters of customers.[368] These customer views were supported by evidence from the Parties which showed that their customers design chips using a design flow made up of a range of suppliers, with the customer choosing the 'best of breed' software at each stage of the design flow.[369] Likewise, evidence from customers indicated that they do not place significant value on a supplier being able to offer a range of software: customers cited a willingness to use smaller suppliers that offered 'best of breed' software with a focus on technical quality.[370] This evidence indicates that customers have a strong preference for using the best quality software and value interoperability between software offered by different suppliers across the various stages of the design flow.[371]

236. On the other hand, third-party evidence indicates that most customers consider price to be very important or important when purchasing products, with several customers indicating that it was important to get the best value for money (ie the best software at the cheapest price possible).[372] Further, around half of customers said they would find a combination of Synopsys and Ansys chip design software attractive.[373] These customers highlighted potential benefits of purchasing at scale and of integration between the software.[374] In addition, around one quarter of

[367] Submission to the CMA from a third party, July 2024 and response to the CMA's questionnaire from a number of third parties, October 2024.
[368] Response to the CMA's questionnaire from a number of third parties, November 2024.
[369] Parties' additional response to the CMA's Issues Letter, 27 November 2024, Figure 6.
[370] Response to the CMA's questionnaire from third parties, November 2024.
[371] The CMA has placed limited weight on the Parties' submission that strength in one chip design software market does not necessarily translate into strength in another related market as there are a range of possible factors that may result in market positions differing as between different related markets, and which do not necessarily preclude conglomerate effects *per se*. The CMA has assessed the evidence on customers' purchasing behaviour and the implications on these theories of harm in the round, along with other evidence.
[372] Response to the CMA's questionnaire from a third party, November 2024.
[373] Response to the CMA's questionnaire from a number of third parties, Q7, November 2024.
[374] Response to the CMA's questionnaire from a number of third parties, November 2024.

customers stated that if, when purchasing Ansys software, they could also get Synopsys chip design software at a discount (or they were integrated into the Ansys software) they would switch from third party software to Synopsys software.[375] This evidence indicates that although customers highly value quality and interoperability between software offered by different suppliers, they also consider price to be an important factor and a material proportion of customers would find a combined offering offered at a discount attractive.

237. In relation to interoperability, the CMA considers that it is not possible based on the evidence it received to wholly exclude the Merged Entity having the technical ability to delay, degrade or remove interoperability with third party software now or in the future. The CMA notes that there may be a wide range of mechanisms through which the Merged Entity could do this, and such strategies could be targeted at particular third-party rivals supplying particular software where there are potential gains to be made (for example, delaying interoperability agreements with specific third-party suppliers) which would not have an impact on Ansys' software used for other types of design (ie non-semi-conductor design). For example:

(a) Several competitors and customers said that the Merged Entity could alter interoperability by creating a proprietary file which software from other providers cannot generate or read (ie third parties could not use the Merged Entity's outputs as inputs).[376] Competitors also considered that interoperability could be affected through altering APIs,[377] as it would be possible for the Merged Entity to close an API or not provide the necessary resources to maintain it (eg in relation to documentation, licensing and support).[378] A customer noted that slower roll out of new features for Ansys software that work with third party software could impact it given that it values software offering the highest quality experience.[379]

(b) A number of competitors submitted that Synopsys has previously delayed interoperability requests.[380]

*Conclusion on ability*

238. The CMA considers that the Merged Entity will have some ability to foreclose rivals in the supply of place and route software, circuit simulation software, parasitic analysis software and timing analysis software globally[381] by leveraging Ansys' strong position in the adjacent markets (the supply of gate-level power integrity analysis for digital and multi-die chips, thermal analysis for multi-die chips,

[375] Response to the CMA's questionnaire from a number of third parties, Q8, November 2024.
[376] Responses to the CMA's questionnaire from a number of third parties, November 2024.
[377] Responses to the CMA's questionnaire from a number of third parties, November 2024.
[378] Response to the CMA's questionnaire from a third party, November 2024.
[379] Note of a call with a third party, September 2024.
[380] Response to the CMA's questionnaire from a number of third parties, November 2024.
[381] For each of the specific chip designs outlined above.

transistor-level power integrity analysis for analog chips, and electromagnetic simulation for analog and multi-die chips globally).

239. In particular, the evidence indicates that Ansys' software are the market leaders and best-in-class; each software faces relatively limited competitive constraints; and customers face high switching costs in relation to this software.

240. The evidence relating to customer preferences for (and thus, the feasibility of) a combined offering is more mixed. On the one hand, customers have a strong preference for using the best quality software and for interoperability between software offered by different suppliers at the various stages of the design flow, which could indicate that the Merged Entity may have limited incentive to engage in a foreclosure strategy. On the other hand, most customers also consider price to be an important factor and a material proportion of customers would be potentially interested in purchasing a combined offering. The CMA has assessed further the feasibility of a combined offering in its analysis of the Merged Entity's incentives below.

241. Finally, in relation to interoperability, the evidence indicates that there may be ways through which the Merged Entity could delay, degrade, or remove interoperability.

*Incentive to foreclose EDA competitors*

242. The CMA has considered the following factors to assess the Merged Entity's incentive to foreclose rivals in the following EDA markets: the global supply of place and route software in each of digital, analog, mixed and multi-die chips; circuit simulation software in each of analog, mixed and multi-die chips; parasitic analysis software in each of digital, analog, mixed and multi-die chips, and timing analysis software in each of digital, analog, mixed and multi-die chips:

(a) The extent of potential gains and losses, focussing on customer preferences, such as the extent to which customers have an interest in purchasing the products in these focal markets alongside RedHawk/RedHawk-SC/RedHawk SC-ET/Totem/HFSS; and,

(b) The business strategy of the Merged Entity.[382]

243. The Parties submitted that the Merged Entity will have no incentive to foreclose rivals as a foreclosure strategy would involve substantial losses given that if it were to attempt to reduce or remove interoperability its software would become less attractive to customers, and both rivals and customers could deploy effective counterstrategies (such as workarounds).[383] The Parties further submitted that the value of Ansys' software depends on the independence of the software to work with third party software, the Parties and their rivals offer software on a standalone

[382] CMA129, paragraph 7.34.
[383] FMN, paragraphs 19.31 onwards.

basis, and customers and competitors could take actions to retaliate against any foreclosure strategy.[384]

*The extent of potential gains and losses*

244. The CMA has first focussed on evidence relating to whether customers could be encouraged to purchase a combined bundle of Synopsys and Ansys software and then on how customers that face delayed, degraded or removed interoperability between the RedHawk software/HFSS and rival software to Synopsys' would respond.[385] The CMA has then considered the sizes of the relevant focal markets and the evidence it has gathered in relation to Synopsys' position in each of these markets.

245. The CMA notes the evidence, described above, that customers have a strong preference for using the best quality software and for interoperability between software offered by different suppliers across the various stages of the design flow. The evidence on potential gains and losses is consistent with these preferences. When asked how they would respond to the delaying, degrading, or removal of interoperability between the RedHawk software/HFSS and the software of Synopsys' rivals, the majority of customers indicated that they were more likely to switch away from the RedHawk software/HFSS to rival software in the adjacent markets that offered better interoperability with rival software in the focal markets than they were to switch to Synopsys' software that interoperate with the RedHawk software/HFSS.

(a) In the event of interoperability between Ansys' RedHawk software/HFSS software and Synopsys' rivals' software being delayed or degraded, three times more customers said that they would switch away from RedHawk to a rival software than switch from a third-party software in a focal market to a Synopsys software. In relation to HFSS, nearly three times more customers said that they would switch away from HFSS to a rival software than switch from a third-party software in a focal market to a Synopsys software.

(b) Further, in the event of interoperability being delayed or degraded, the large majority of customers said that they would neither switch away from Redhawk/HFSS or switch to a Synopsys software. These customers said that they would either develop their own workarounds to manage the reduced interoperability or they would continue to use their existing workflow despite the reduced interoperability, ie continue to be customers of rivals of the Parties, with no effect resulting on the use of rival software.

(c) In the event of interoperability between Ansys' RedHawk software/HFSS software and Synopsys' rivals' software being removed, nearly double the

[384] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 7.8.
[385] The CMA did not gather evidence in this respect specifically relating to Totem, but considers customers' feedback in relation to their willingness to switch from RedHawk/HFSS to be broadly applicable to Theory of Harm 7c given Ansys' strength in this market as well as in the adjacent markets considered at Theory of Harms 7a and b.

number of customers said that they would switch away from RedHawk to a rival software than switch from a third-party software to a Synopsys software in the focal market. In relation to HFSS, over double the number of customers said that they would switch away from HFSS than switch from a third-party software to a Synopsys software in the focal market.

246. The relevant customers explained their reasons for either switching away from RedHawk/HFSS, developing workarounds, or continuing to use third party software in the focal markets despite delayed or degraded interoperability:

(a) Customers, including those in Synopsys' and Ansys' top 20 customers, as well as a number of smaller customers, noted that delaying, degrading, or removing the interoperability of Ansys' software would 'destroy' the utility of the Ansys software, given customer needs for these software to work with other 'best of breed' software and stated that such a strategy would not make 'commercial sense' for the Merged Entity, and would 'appear contrary to the Merged Entity's commercial interests,' supporting the Parties' submissions that Ansys' software need to be independent and work with third party software.[386] These customers also noted that interoperability was a 'cornerstone' of the chip design industry and they would 'oppose any strategy to limit' interoperability between software.[387]

(b) Customers, including a number of Synopsys' and a number of Ansys' top 20 customers, as well as a number of smaller customers, noted that they had the capability to develop workarounds and their own internal solutions to any delaying or degrading of interoperability.[388] However, some other large customers did raise doubts about their ability to develop their own workarounds.[389] One smaller customer also had doubts about its ability to create its own workaround solutions noting that the features that would allow it to do so may not exist.[390]

(c) Customers who stated that they would continue to use third party software despite delayed or degraded interoperability noted the costs of changing workflows that are already in place and described their willingness to do this (sometimes in conjunction with workarounds). These customers included some of the Parties' top 20 customers as well as smaller customers.[391] Some larger customers noted that they may do this whilst exploring alternatives to RedHawk/HFSS and transitioning away from these software for new projects.[392]

(d) Customers adopt multi-vendor strategies and use multiple vendors for software with the same functionality. One large customer of the Parties noted

[386] Response to the CMA's questionnaire from a number of third parties, November 2024.
[387] Submission to the CMA from a number of third parties, May-August 2024.
[388] Response to the CMA's questionnaire from a number of third parties, November 2024.
[389] Response to the CMA's questionnaire from a number of third parties, November 2024.
[390] Note of call with a third party, September 2024.
[391] Response to the CMA's questionnaire from a number of third parties, November 2024.
[392] Response to the CMA's questionnaire from a number of third parties, November 2024.

that this allowed customers to switch between software in the event that any particular supplier attempted to take advantage of a strong market position. This customer noted that this strategy had been successful in ensuring that interoperability between software was maintained and allowed customers access to 'best of breed' software.[393] This strategy is employed by customers of all sizes: a number of customers, including a top 20 customer of both Parties, as well as smaller customers, noted that they have a multi-vendor strategy.[394] Further, in response to the CMA's questionnaire, around half of customers stated that having a diversity of suppliers or a multi-vendor strategy was important or very important to them in informing their purchasing strategy.[395] Consistent with this, the Parties provided evidence that indicated that around [✂] of RedHawk's largest customers also already use Voltus.[396]

(e) As noted above, the CMA gathered evidence that switching away from Ansys software (RedHawk/RedHawk-SC, RedHawk-SC ET, Totem and HFSS) in the adjacent markets is difficult. However, the CMA also gathered some evidence that switching to Synopsys software in the focal markets may also be difficult or not the preference of customers, thus limiting the Merged Entity's gains. For example, one customer noted that their choice of place and route software was more important than sign-off options, and they would not switch to Synopsys from their preferred place and route software,[397] whilst another customer noted that switching to Synopsys would not be an easy task and would be expensive and take a long time.[398]

247. The CMA notes that the evidence relating to customer responses set out above is consistent with evidence that the current market practice is, as submitted by the Parties, for chip design software suppliers to offer software on a standalone basis. One competitor noted that whilst it has 'best of breed' software, a key selling point is that it 'integrates well with other EDA [software] and design environments to give a seamless workflow for designers'.[399] Another major competitor with a range of software (many of which were identified by customers as alternatives to Ansys' software) noted that whilst it offers integrated software, it also offers all software on a standalone basis in order to 'cover the different needs of customers'.[400] Synopsys submitted that it has, throughout its history, offered its software on a standalone basis,[401] and this is also the case for software that it has acquired.[402]

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[393] Note of call with a third party, July 2024.
[394] Response to the CMA's questionnaire from a number of third parties, November 2024.
[395] Response to the CMA's questionnaire from a number of third parties, November 2024.
[396] Synopsys' submission on why Synopsys could not leverage RedHawk to harm competitors, 5 September 2024, Table 1.
[397] Response to the CMA's questionnaire from a number of third party, November 2024.
[398] Response to the CMA's questionnaire from a number of third party, November 2024.
[399] Submission to the CMA from a third party, April 2024.
[400] Submission to the CMA from a third party, April 2024.
[401] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 7.8.
[402] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 7.31.

248. Given the above, the CMA considers that the potential losses to the Merged Entity from engaging in a foreclosure strategy could be significant. Whilst the CMA has not quantified these losses, it notes that around [✂] of RedHawk's revenues comes from customers that use it alongside [✂] place and route software [✂].[403]

249. In relation to potential gains, the CMA notes that although the focal markets appear to be relatively large (the estimated global market size in 2023 for place and route software was estimated to be worth £[✂] million, circuit simulation £[✂] million and timing analysis £[✂] million)[404] and the position of Synopsys in these markets is relatively strong (for example, the evidence currently available to the CMA indicates that in relation to place and route software Synopsys and Cadence are the 'top suppliers'[405] and in relation to simulation software Synopsys' SPICE is the market leader, followed by Cadence),[406] the number of customers stating that they would switch to Synopsys' software was relatively small (see discussion earlier in this section), limiting the potential gains for the Merged Entity.

*Business strategy of the Merged Entity and other costs and benefits*

250. The CMA has considered the extent to which there is evidence that the Merged Entity's business strategy involves a foreclosure approach, whether the Merged Entity has a history of engaging in any such behaviour, and the extent to which the Merger rationale involves plans to engage in any foreclosure (either through bundling or delaying, degrading, or removing interoperability).[407] The CMA has also considered whether there are other costs and benefits to the Merged Entity of engaging in such a strategy, particularly in light of potential future developments and changes in customer demands.

251. In the future, the integration between S&A and EDA software is expected to increase in importance as multi-die chip design is adopted by more customers. Integration between software is important to ensure that design errors with material consequences are picked up as early as possible in the design process. As such, customer demand for integrated software is expected to increase in the future, with one customer stating that in the future for multi-die chips they would prefer an integrated 3DIC software, as a higher degree of integration reduces the need for engineers to make manual fixes.[408] In considering the Merged Entity's business strategy, therefore, the CMA has had particular regard to how the market may evolve and the Parties' Merger rationale, and placed less weight on past behaviour as a guide to the Merged Entity's medium to long term strategic incentives and future behaviour.

252. In this context, the CMA notes that it has received some allegations that that Synopsys may have, to some extent, attempted to delay, degrade or remove

[403] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 7.19.
[404] Annex RFI6Q4.1 to the FMN, Parties' estimates. The CMA does not have equivalent estimates for parasitic analysis.
[405] For example, Submission to the CMA from a third party, June 2024.
[406] Note of a call with a third party, July 2024.
[407] CMA129, paragraph 7.34a.
[408] Note of call with a third party, October 2024.

interoperability in the past. However, the CMA has, in the absence of any clear pattern of behaviour by Synopsys in this respect, placed limited evidentiary weight on these claims.[409]

253. The CMA notes that the rationale of the Merger is focussed on providing 'comprehensive… solutions through deeper technical integration,' indicating that the Parties consider that an integrated combined offer will be an attractive proposition to customers. As noted previously, Synopsys considers Ansys' software are key to achieve this aim. Given this, the strategy of the Merged Entity appears to be focussed on providing an offering with deeper integration between Synopsys' and Ansys' software. The CMA has not seen any evidence from the Parties' internal documents which indicate that they would delay, degrade, or remove interoperability, or attempt to foreclose rivals. A large number of the Parties' top customers welcomed deeper integration between Synopsys and Ansys software. A significant number of the Parties' top customers provided reasoned submissions expressing support for the Merger. These customers welcomed the prospect of Synopsys natively integrating Ansys' S&A capabilities into its EDA software flow (with several expressing that this would make Synopsys better able to compete with Cadence's current offering),[410] and at the same time expressed confidence that Synopsys would be committed to maintaining interoperability between its software and third-party software. Given the level of sophistication of these customers, their importance to the Parties, and their knowledge of the relevant markets, the CMA has placed material weight on these views, as well as those of a range of smaller customers, when considering the Merged Entity's likely strategy, and considered them in the round, whilst also being mindful of the evolving nature of the relevant markets and accordingly, of the Merged Entity's future incentives. The CMA has also placed weight on the fact that following extensive third party engagement in which the CMA contacted hundreds of customers who ranged broadly in size and importance to the Parties, the vast majority of customers expressed either positive or neutral views regarding the Merger, and that of the concerns noted at paragraph 200 that were expressed by customers, none were supported by reasoning and represented isolated comments.

*Conclusion on incentives*

254. On the basis of the evidence set out above, and considered in the round, the CMA considers that the Merged Entity will not have the incentive to foreclose rivals in the supply of place and route software for digital, analog, mixed and multi-die

[409] Response to the CMA's questionnaire from a number of third parties, October 2024. Third party responses to the CMA's Request for Information, 15 November 2024, (**RFI 3**). The CMA notes that several of the ad-hoc examples provided by third parties were not substantiated with evidence, and where specific examples were raised by third parties, such as Synopsys' acquisition of Tweaker, Synopsys maintained that it has continued to support interoperability between software it has acquired with third-party software. Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 7.31.
[410] The CMA notes that Cadence has previously stated that the Parties are 'trying to react to what we [Cadence] did like 6 years ago' (CEO of Cadence, Anirudh Devgan, JPMorgan TMT Conference, 21 May 2024) [✂]. [✂].

chips, circuit simulation software for analog, mixed and multi-die chips, parasitic analysis software digital, analog, mixed and multi-die chips and timing analysis software for digital, analog, mixed and multi-die chips globally given consistent evidence from customers that any foreclosure strategy would lead to material losses and only limited gains for the Merged Entity. The CMA notes that whilst the Merged Entity may develop better integrated software in the future (which would benefit customers), the evidence indicates that it will still have an incentive to ensure that this software remains interoperable with third party software.

255. The CMA has not considered the effect on competition of a potential foreclosure strategy given its finding that the Merged Entity is unlikely to have the incentive to foreclose rivals.

*Conclusion*

256. Given the above, the CMA currently considers that whilst the Merged Entity would have some ability to foreclose rivals in the focal markets by leveraging its position in adjacent markets in which Ansys has market power, it would not have the incentive to do so. In particular, consistent evidence from customers indicates that any foreclosure strategy would lead to material losses and only limited gains for the Merged Entity. Therefore, the CMA believes that the Merger does not give rise to a realistic prospect of an SLC as a result of conglomerate effects in the supply of place and route software for digital, analog, mixed and multi-die chips, circuit simulation software for analog, mixed and multi-die chips, parasitic analysis software for digital, analog, mixed and multi-die chips or timing analysis software for digital, analog, mixed and multi-die chips globally.

*Theory of Harm 8: Conglomerate effects resulting in the foreclosure of S&A / EDA software rivals by leveraging Synopsys' position in Design IP globally*

257. A conglomerate relationship also arises between the Parties as Synopsys supplies Design IP and Ansys supplies S&A and EDA software, all of which are purchased by common customers. Synopsys offers Design IP in the form of pre-designed building blocks of chip components with standardised functionality, which customers license and incorporate into their chip designs.[411] The CMA therefore considered whether the Merged Entity could use its position in a number of possible markets in the global supply of Design IP to foreclose rivals of primarily, Ansys in the supply of S&A (and to a more limited extent, EDA) software.[412] Specifically, in light of Synopsys' substantial position in the supply of Design IP

[411] FMN, paragraph 3.1. Synopsys' portfolio of IP products includes logic libraries, embedded memories, analog IP, wired and wireless interface IP, security IP, and embedded processor IP.
[412] The CMA has focused its analysis on the impact of the Merger on primarily Ansys' rivals given Synopsys already offers both Design IP and various types of EDA (and to a lesser extent, S&A) software globally. Given the lack of concerns in relation to this theory of harm on any basis, the CMA has not concluded on the exact scope of the markets in which there are rivals to Ansys' software that could be harmed by any foreclosure strategy.

globally,[413] the CMA has considered whether the Merged Entity could link sales of the Parties' Design IP and S&A/EDA products together (for example, through bundling or tying), to foreclose S&A/EDA rivals from competing effectively.[414]

258. The CMA received comments from a small number of third parties that Synopsys could use its strong position in Design IP to engage in bundling practices so as to 'lock in' customers to the Merged Entity's software,[415] with one competitor stating that Synopsys has previously offered customers discounted chip design software when they purchase Synopsys' Design IP.[416] However, the evidence the CMA received in its investigation indicates that the large majority of customers do not acquire Design IP and software products together, as Design IP tends to be purchased for specific projects, whilst software products are purchased and contracted for over different set time periods. Customers noted that given the different purchasing cycles, they do not see an opportunity to benefit from purchasing the two products together.[417] In addition, the large majority of customers did not consider it important that their suppliers of software products also offered Design IP, preferring high-quality, 'best of breed' software products (see Industry overview section) regardless of those suppliers' wider offering, with most customers stating that they would not purchase bundles where Synopsys' or Ansys' software products were only available with Design IP as they preferred to keep their independence in choice of software products.[418]

259. Accordingly, the CMA did not consider that software rivals would be deprived of a large volume of sales if the Merged Entity were to bundle/tie its offering. Even if the Merged Entity pursued a bundling/tying strategy, customers would be unlikely to switch from their current software supplier, which would limit the profitability of a foreclosure strategy. The large majority of third party respondents did not raise concerns regarding any linkage of Design IP and software products.

260. For the reasons outlined above, the CMA believes the Merged Entity would have neither the ability nor the incentive to leverage its position in Design IP globally to foreclose rivals of S&A and/or EDA software through a bundling/tying strategy. Therefore, the CMA believes that the Merger does not give rise to a realistic prospect of an SLC as a result of conglomerate effects in the supply of any EDA or S&A software globally.

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[413] For categories where Synopsys estimated its share to be higher than 20%, Synopsys estimated its share of supply in the various categories of Design IP globally to be: (i) [50-60]% in embedded memories; (i) [30-40]% in physical libraries; and (iii) [60-70]% in wired interface IP (Parties' response to the CMA's Request for Information, 14 June 2024, Annex Q17.1, Parties' estimates).
[414] CMA129, paragraph 7.33b.
[415] Submissions to the CMA from a third party, April 2024; response to the CMA's questionnaire from a third party, October 2024.
[416] Third party response to the CMA's Request for Information,15 November 2024, paragraph 28. However, the CMA has not seen any evidence that any previous instances of Synopsys providing Design IP bundled with its own software products has led to software competitors being unable to compete and being foreclosed.
[417] Response to the CMA's questionnaire from a number of third parties, October 2024.
[418] Response to the CMA's questionnaire from a number of third parties, October 2024.

## Loss of future competition

*Market context*

261. As discussed in paragraph 45, R&D is an important element of competition for both EDA and S&A suppliers. The CMA considers that the Parties are among a number of suppliers that play key roles in driving innovation for multi-die chip designs. All competitors that responded to the CMA's questionnaire said that both Synopsys and Ansys are important in driving innovation for software used to design 3DIC chips.[419] Cadence and Siemens also appear to invest heavily in R&D.[420] Further, as discussed in paragraphs 21 to 22, the Parties' internal documents show that they have been monitoring areas of future growth and developments in multi-die chip design. Synopsys considers that the 'key relevant players' in developing software to design multi-die chips are the [✂], [✂], [✂], [✂] and [✂].[421]

262. The CMA considers that recent developments in chip design are important background to the assessment of competitive dynamics within this sector. As noted above and in the Merger rationale section, multi-die chip designs are an increasingly important market trend. Multi-die chips have complex architecture in comparison to other types of chips. This means that the signoff stage is particularly important when designing a multi-die chip to ensure that the chip will perform as expected. In response to customer demand, and as noted at paragraph 58, 'shift left' has meant that S&A software is increasingly being used earlier rather than later in the chip design flow.[422] Ansys, as noted above in the Conglomerate effects section, is strong in the supply of a number of signoff software including (i) RedHawk-SC ET, which is used for thermal analysis, which ensures multi-die chips allow heat to dissipate, (ii) HFSS, which is used for electromagnetic simulation analysis , which verifies how a chip will respond to electromagnetic signals and (iii) RedHawk and RedHawk-SC for gate-level power integrity analysis, which verifies the power distribution of a chip.

263. Synopsys' internal documents show that it has been monitoring developments in multi-die chips and has been developing certain functionality for use in its software for multi-die chips including [✂] analysis, [✂] and [✂] analysis.[423] The CMA has considered whether these plans would lead Synopsys to compete with Ansys' signoff software in the future.

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[419] Response to the CMA's questionnaire from a number of third parties, October 2024, question 11.
[420] Response to the CMA's questionnaire from a number of third parties, October 2024, question 4.
[421] Synopsys' internal document, Annex SNPSCMA-00011245, '[✂]', 1 March 2023, slide 29.
[422] See also FMN, paragraph 9.
[423] Synopsys' internal document, Annex SNPSCMA-00011245, '[✂]', 1 March 2023, slide 2. Synopsys' internal document, Annex SNPSCMA-00008208, '[✂]', 16 Dec 2022, slide 21.

*Future competition*

264. Unilateral effects may arise from the elimination of potential competition.[424] Potential competition refers to competitive interactions involving at least one firm that has the potential to enter or expand in competition with other firms.[425] To this end, the CMA considers whether a merger could substantially lessen competition where, absent the merger, entry or expansion by one or both merger firms could have resulted in new or increased competition between them.[426] Mergers involving a potential entrant can lessen competition in different ways. A merger involving a potential entrant may imply a loss of the future competition between the merger firms after the potential entrant would have entered or expanded.[427]

265. In assessing whether a merger involving potential entry or expansion will lead to a loss of future competition between the merger firms, the CMA will consider evidence in relation to:[428]

(a) whether either merger firm (or both merger firms) would have entered or expanded absent the merger; and

(b) whether the loss of future competition brought about by the merger would give rise to an SLC, taking into account other constraints and potential entrants / expansion.

266. The CMA has focussed its assessment on the potential loss of future competition as the evidence it has seen demonstrates that, as part of its ongoing efforts to address customer demands arising from the trend towards multi-die chip designs, Synopsys has a number of R&D projects to develop [✂]. The CMA has [✂] considered whether the Merger may lead to a loss of future competition in the following markets (all of which fall into, broadly speaking, the category of 'multi-die signoff'):

(a) supply of thermal analysis for multi-die chips globally (considered in **Theory of Harm 9**);

(b) supply of electromagnetic simulation analysis for multi-die chips globally (considered in **Theory of Harm 10**); and

(c) supply of gate-level power integrity analysis for multi-die chips globally (considered in **Theory of Harm 11**).

267. The CMA has focused on whether the Merger would lead to a loss of future rather than dynamic competition in relation to the three markets described above as nothing in Ansys' internal documents indicated that it perceived there to be, or was

[424] CMA129, paragraph 5.1.
[425] CMA129, paragraph 5.1.
[426] CMA129, paragraph 5.1.
[427] CMA129, paragraph 5.2.
[428] CMA129, paragraph 5.7.

reacting to the possibility of, any future [✂] forthcoming from Synopsys in these, or other, markets (for example, in terms of its innovation efforts).[429]

*Synopsys' submissions*

268. Synopsys submitted that it does not have plans, or the ability or incentive to enter and compete in S&A markets where Ansys is active, including those listed in paragraph 266.[430] In particular:

(a) Synopsys' three R&D projects do not and would not compete with Ansys because these projects are not intended to develop [✂] signoff S&A products, but rather to [✂] the [✂] of Synopsys' existing EDA software.[431] These projects seek to fulfil customers' increasing needs for [✂] capabilities throughout the [✂] (particularly for multi-die chip designs) and therefore serve a use case that Ansys does not provide and could not provide in the future – namely, [✂].[432] These projects will therefore help Synopsys compete better with [✂] and [✂], not to compete with Ansys;[433]

(b) developing multi-die signoff capabilities which Ansys (and others) offer would require resources, expertise and technology that Synopsys [✂], and would [✂] in a competitive [✂];[434]

(c) Ansys' signoff software is not suited for the [✂] analysis that Synopsys' research projects will deliver because it is [✂] and [✂];[435] and

(d) even if Synopsys had the ability and incentive to compete with Ansys in S&A (which it does not), the Merged Entity would continue to face strong competitive constraints in S&A, such that any (hypothetical) loss of competition in S&A would have no material effect on the competitive dynamics.[436]

[429] Mergers can reduce the dynamic competitive interactions between an existing supplier and a dynamic competitor, as a merger could lead the existing supplier to reduce its efforts in the present to protect against the possible impact of the dynamic competitor, as any future loss of sales to the dynamic competitor would not reduce the profits of the merged entity (CMA129, paragraph 5.19(a)).
[430] Synopsys' submission on potential future competition, 8 November 2024, paragraph 1.2.
[431] Synopsys' submission on potential future competition, 8 November 2024, paragraphs 1.3 and 1.4. Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.2.
[432] Synopsys' submission on potential future competition, 8 November 2024, paragraphs 5.1 and 5.2. Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraphs 8.3 and 8.4.
[433] Synopsys' submission on potential future competition, 8 November 2024, paragraph 2.4. Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.5.
[434] Synopsys' submission on potential future competition, 8 November 2024, paragraphs 5.1 and 5.2. Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.6.
[435] Synopsys' submission on potential future competition, 8 November 2024, paragraph 2.9.
[436] Synopsys' submission on potential future competition, 8 November 2024, paragraph 1.6.

*Theory of Harm 9: Loss of future competition in thermal analysis for multi-die chips globally*

*Project [✂]*

269. Project [✂] is Synopsys' R&D project relating to [✂] multi-die chips. Ansys currently competes in thermal analysis via RedHawk-SC ET. Synopsys does not currently offer its own thermal analysis software but has developed workflows with Ansys' RedHawk-SC ET.

*Synopsys' submissions*

270. In addition to Synopsys' general submissions in relation to all three of its R&D projects set out at the beginning of this section, Synopsys submitted specifically on Project [✂] that:

    (a) Project [✂] is not intended to be launched as a [✂] product, but rather introduced to provide [✂] capabilities for Synopsys' EDA software. It will [✂] analysis capabilities to Synopsys' EDA software to provide [✂]-aware and improved [✂] for multi-die designs;[437] and

    (b) Project [✂] is not and was never intended to be a [✂] analysis multi-die signoff software product; [438]

    (c) Project [✂] does not and could not compete with Ansys as it has different areas of focus; [439]

    (d) Synopsys lacks the ability and incentive to develop a [✂] analysis software product in a sufficiently [✂] that would compete with Ansys; [440] and

    (e) Project [✂] was [✂] tested in [✂] with several customers ([✂] and [✂]). It entered the [✂] phase (testing the product's capabilities [✂]) with one customer ([✂]) in [✂]. [✂] validated Project [✂] in [✂], and it is expected to launch, at the earliest, in the second half of [✂] but this is '[✂]'.[441]

*CMA assessment*

271. While the CMA notes that Project [✂] has reached a relatively well-developed stage of pipeline development, with Synopsys having tested and requested feedback from [✂] customers and gained at least [✂] foundry certification,[442] the CMA considers that the evidence, taken in the round, does not indicate that

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[437] Synopsys' submission on potential future competition, 8 November 2024, paragraph 2.4.
[438] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.10.
[439] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraphs 8.11 and 8.12.
[440] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.14.
[441] Synopsys' response to the CMA's section 109 Notice, 11 July 2024, Table 3.
[442] Synopsys' internal documents, Annex SNPSCMA-00010347, '[✂]', 31 January 2024, slide 5. Synopsys entered the [✂] phase ([✂] the products capabilities [✂]) with one customer ([✂]) in [✂]. The Parties' submissions and several Synopsys' internal documents show that Project [✂] had gained foundry certification [✂] and was working to gain a certification from [✂]. See Synopsys' internal document, Annex SNPSCMA-00011276, '[✂]', 30 January 2024, slide 22; Synopsys' internal document, Annex PN RFI 4 - Q.16-004, '[✂]', March 2024, slide 5 and 10, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, '[✂]', 26 July 2024.

Synopsys was seeking to develop a software product that competes with Ansys' RedHawk-SC ET product. Although several of Synopsys' internal documents indicate some degree of [✂] between Project [✂] and Ansys' RedHawk-SC ET, and [✂],[443] a number of documents suggest that Project [✂] and RedHawk-SC ET are complementary as Project [✂] is intended for [✂] whereas RedHawk-SC ET is for signoff analysis (which aligns with the Parties' submissions).[444]

272. A range of further evidence relating to the project suggests that there are key differences between [✂] and Ansys' software which limit the extent to which customers would be able use these software products as substitutes. In some internal documents, Synopsys notes that [✂] would enable customers to conduct (i) [✂] which allows [✂] analysis in Synopsys' [✂] analysis product, (ii) [✂] using [✂] and [✂] which allows [✂] analysis in Synopsys' [✂], and (iii) [✂] analysis using [✂] and [✂] which allows [✂] and [✂] analysis respectively.[445] The CMA understands that Ansys' RedHawk-SC ET does not allow customers to conduct these functions and has not seen any evidence to indicate otherwise.

273. In particular, the CMA has not seen any evidence to indicate that Ansys' RedHawk-SC ET can be used [✂] in the chip design flow by customers and that this software can be combined with [✂] which have a [✂] to enable [✂] analysis (including for [✂] or [✂] analysis software).

274. One Synopsys internal document indicates that [✂] signoff analysis does not currently exist (and as such is not provided by Ansys) and Project [✂] would aim to provide this functionality.[446] The CMA has seen limited evidence to suggest that Project [✂] might be developed into a [✂] signoff product.[447] Instead, the CMA has seen one internal document which highlights that a new Synopsys [✂] product would not be [✂], and another early-stage document which characterises [✂] as an opportunity to enter a new market 'while [✂]'.[448] Another later stage document from 2023 notes in relation to each of Project [✂], [✂] and [✂] that these pose 'no direct [✂] to Ansys' [✂]'.[449]

275. Based on the above, the CMA believes that the available evidence does not indicate that Project [✂] would compete with Ansys' RedHawk-SC ET. The CMA also notes that, as set out in the assessment of Theory of Harm 7b, RedHawk-SC

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[443] Synopsys' internal document, Annex SNPSCMA-00011245, '[✂]', 1 March 2023, slide 17; Synopsys' internal document, Annex SNPSCMA-00006295, '[✂]', 17 March 2022, slide 6; Synopsys' internal documents, Annex PN RFI 4 - Q.16-001.pdf, '[✂]', 14 November 2022 slide 12, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, '[✂]', 26 July 2024; Synopsys' internal document, Annex SNPSCMA-00011276, '[✂]', 30 January 2024, slide 16.
[444] Synopsys' internal document, Annex Q9(SNPS) – 001, '[✂]', 25 October 2023, slide 2
[445] Synopsys' internal document, Annex PN RFI 4 - Q.16-004, '[✂]', March 2024, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, [✂]', 26 July 2024. Synopsys' internal document, Annex SNPSCMA-00011276, '[✂]', 30 January 2024, slide 8. Synopsys' internal document, Annex SNPSCMA-00011194, '[✂]', 14 November 2022, slide 4.
[446] Synopsys' internal document, Annex SNPSCMA-00011276, '[✂]', 30 January 2024, slide 8.
[447] Synopsys' internal documents, Annex Q8(SNPS) – 005, '[✂]', 26 October 2023, slide 31.
[448] Synopsys' internal documents, Annex PN RFI 4 - Q.16-001.pdf, '[✂]', 14 November 2022, slide 18; Synopsys' internal document, SNPSCMA-00003598, '[✂]', 28 June 2021, slide 8.
[449] The document goes on to note that the position (as regards lack of direct competitive threat to Ansys) could change after its planned [✂] of [✂]. The CMA's assessment of the impact of Synopsys' acquisition of certain [✂] assets is considered at Theory of Harm 11 below. Synopsys' internal document, SNPSCMA-00011245, '[✂]', 1 March 2023, slide 23.

ET will continue to face, post-Merger, a significant constraint from Cadence and a relatively weak constraint from Siemens.

276. Accordingly, the CMA found that the Merger does not give rise to a realistic prospect of an SLC as a result of a loss of future competition in the supply of thermal analysis for multi-die chips globally.

*Theory of Harm 10: Loss of future competition in electromagnetic simulation analysis for multi-die chips globally*

277. Electromagnetic simulation software is an important part of the signoff stage of chip design, as it verifies how a chip will respond to electromagnetic signals, in particular, to ensure that the chip will operate as intended and not be susceptible to, or create, electromagnetic interference.[450]

278. Ansys currently competes in the supply of electromagnetic simulation analysis globally via HFSS for 3DIC chip design flows and RaptorH for 2.5D chip design flows.[451] Synopsys does not currently offer electromagnetic simulation analysis but instead has workflows between Ansys' HFSS and RaptorH and its wider chip design software to offer this functionality.

279. In 2023 Synopsys acquired certain assets from [✂] (a [✂]) relating to its [✂] analysis software [✂] and [✂]. This included:

(a) The [✂] for [✂] and [✂] for use in Synopsys' [✂] (which would allow Synopsys to develop its own [✂] analysis software);

(b) The rights to sell [✂] and [✂] products outside of [✂]; and

(c) The rights to acquire [✂] entity and its existing [✂].[452]

280. [✂] and [✂] have functional overlaps with Ansys' HFSS and Raptor H respectively. However, they generated very limited revenue outside of [✂] in 2023.[453]

281. The CMA considered whether Synopsys would compete with Ansys in the supply of electromagnetic simulation analysis globally in the future as a result of its R&D **Project** [✂], which includes (i) Synopsys' rights to sell [✂] and [✂] (outside of [✂]), and (ii) Synopsys' potential development of its own [✂] analysis software.

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[450] See https://www.ansys.com/products/electronics/ansys-hfss?utm_campaign=product&utm_medium=paid-search&utm_source=google&utm_content=digital_electronics_copr15el_contact_contact-us_hfss-electronics-brand-search_1a_en_global&campaignid=7013g000000cXBXAA2&utm_term=ansys%20hfss&gad_source=1&gclid=EAIaIQobChMIk7jspNDtiQMVLqJQBh2jvh50EAAYASAAEgKcvPD_BwE

[451] RaptorH is an electromagnetic simulation software that offers customers the choice between using HFSS or RaptorX. As noted in the Background and nature of competition section, 2.5D and 3D ICs refer to different layered chip architectures. 2D ICs incorporate chips next to each other on the same surface (substrate), 2.5D ICs incorporate chips placed next to each other on the same surface (substrate), but separated by an interposer and 3D ICs stack chips on top of each other, separated by several interposers. FMN, paragraph 30.

[452] FMN, paragraph 16.32, footnote 418.

[453] FMN, paragraph 16.32, footnote 418.

*Synopsys' submissions*

282. In addition to Synopsys' general submissions regarding all three of its R&D projects as set out at the beginning of this section, Synopsys submitted specifically on Project [✂] that:

(a) Project [✂] is not intended to lead to the launch of a [✂] product (ie a [✂] software), but rather to [✂] capabilities to Synopsys' [✂] software, and would offer complementary capabilities to Ansys' signoff software;[454]

(b) The rights to sell [✂] and [✂] as part of Project [✂] will not enable Synopsys to compete with Ansys in the future as they are not Synopsys' products;[455]

(c) [✂] and [✂] do not compete closely with Ansys' HFSS and Raptor X respectively as the software have different areas of focus;[456]

(d) Synopsys lacks the ability and incentive to develop an [✂] signoff software in a sufficiently [✂];[457] and

(e) Project [✂] was [✂] tested in [✂]. This testing focused on adjusting the [✂] received from [✂] and integrating it into Synopsys' [✂] and [✂]. It has not been tested with customers and the next stage of testing [✂].[458]

*CMA assessment*

283. The CMA considers that the evidence does not indicate that Project [✂] would compete closely with Ansys' signoff software.

284. As regards [✂] and [✂], the evidence does not indicate overall that the [✂] and [✂] products compete closely with Ansys' offering. Although certain of Synopsys' internal documents indicate it considers these products to [✂] in this market,[459] Ansys' internal documents do not suggest that it monitors [✂] or other [✂] products as part of its competitive monitoring in the ordinary course of business. Similarly, no customers mentioned either [✂] or [✂] as being alternatives to Ansys' existing offerings in this market. The CMA further notes that Synopsys'

[454] FMN, paragraph, 16.36-37, and Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.17.
[455] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.20.
[456] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.20.
[457] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.21.
[458] Synopsys' response to the CMA's section 109 Notice of 11 July 2024, 26 July 2024, Table 3.
[459] Synopsys' internal document, Annex PN RFI4 – 16-009, '[✂]', May 2023, slide 8, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, '[✂] RFI 4 - Response Tranche 2', 26 July 2024. Synopsys' internal document, Annex PN RFI4 – 16-006, '[✂]', July 2023, slides 24, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, '[✂] RFI 4 - Response Tranche 2', 26 July 2024. Synopsys' internal document, Annex PN RFI4 – 16-006, '[✂]', July 2023, slide 24, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, '[✂] RFI 4 - Response Tranche 2', 26 July 2024. Parties' response to the CMA's Issues Letter, 27 November 2024, paragraph 8. Synopsys' internal document, Annex Q9(SNPS) – 035, '[✂]', April 2023, slide 18. Synopsys' internal document, Annex SNPSCMA-00011245, '[✂]', 1 March 2023, slide 23.

capabilities with respect to [✂] and [✂] are limited by the fact that [✂] and accordingly, does not compete on quality or innovation parameters given, [✂].[460]

285. As regards Synopsys' product development through its [✂], certain of Synopsys' internal documents suggest that its development plans, which appear to be at a [✂] early stage, with no [✂] yet with customers,[461] focus on adding earlier stage [✂] its own existing software which would be [✂] complement rather than a substitute to Ansys' software which are used at [✂] chip design stages.[462]

286. Further, the evidence indicates that the Merged Entity will face strong competitive constraints post-Merger. While Ansys has a strong market position in the supply of electromagnetic simulation for multi-die chips globally, as noted in Theory of Harm 7d, the Merged Entity would face a significant competitive constraint from Cadence, a material constraint from Dassault post-Merger and there is also a tail of smaller competitors, including Siemens.

287. In relation to 2.5D multi-die chips specifically, the evidence indicates that Cadence's EMX exerts a significant constraint on Ansys' RaptorH. One Ansys internal document benchmarks [✂] as a competitor and notes that [✂] of Ansys' customers benchmark RaptorH against [✂].[463] Further, in one internal document Synopsys notes that it considers that [✂] is [✂] the [✂] and that it '[✂]]'.[464]

288. For the reasons set out above, the CMA considers that Synopsys' products under development, which are still at a [✂] early development stage, would not compete with Ansys' products. The CMA also considers that [✂] and [✂] do not compete closely with Ansys' products. Further, the CMA considers that the Merged Entity would face significant and strong competitive constraints from Cadence and Dassault respectively post-Merger.

289. Accordingly, the CMA found that the Merger does not give rise to a realistic prospect of an SLC as a result of a loss of future competition in the supply of electromagnetic simulation analysis for multi-die chips globally.

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[460] The importance of having a specialised engineering and R&D team is further discussed in paragraph 302.
[461] Synopsys' response to the CMA's section 109 Notice of 11 July 2024, 26 July 2024, Table 3. Synopsys' internal document, Annex Q8(SNPS) – 005, '[✂]', 26 October 2023, slide 31. Synopsys' internal document, Annex PN RFI4 – 16-007, '[✂]', April 2023, slide 5, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, '[✂] RFI 4 - Response Tranche 2', 26 July 2024.
[462] Synopsys internal document, Annex PN RFI 4 - Q.16-006, '[✂]', slides 3, 4 and 24, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, '[✂] RFI 4 - Response Tranche 2', 26 July 2024. Synopsys' internal document, Annex PN RFI 4 - Q.16-007, '[✂]', Apr 2023, slide 5, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, '[✂] RFI 4 - Response Tranche 2', 26 July 2024.
[463] Ansys' internal document Annex s.109(1)(ANSS)-2210, '[✂]', 25 July 2024, slide 97.
[464] Synopsys' internal document, Annex PN RFI4 – 16-009, '[✂]', May 2023, slide 8, contained in Synopsys' internal document, Annex RFI4Q15(SNPS) – 14, '[✂]', 26 July 2024.

*Theory of Harm 11: Loss of future competition in gate-level power integrity analysis for multi-die chips globally*

*Project [✂]*

290. Project [✂] is Synopsys' R&D project relating to [✂] analysis for multi-die chips. Ansys currently competes in gate-level power integrity analysis via RedHawk and RedHawk-SC.[465] Synopsys does not currently offer its own gate-level power integrity analysis product but has developed workflows with Ansys' RedHawk/RedHawk-SC.

291. Gate-level power integrity analysis software verify the power distribution of a chip design to ensure that there are no issues with voltage drop or other factors that could affect the reliability of the design and are therefore an important part of the signoff stage.

*Synopsys' submissions*

292. In addition to Synopsys' general submissions on all three of its R&D projects (set out at the beginning of this section), in relation to Project [✂] specifically, Synopsys submitted that:

(a) Project [✂] is not intended to lead to the launch of a [✂] product, but rather introduced as [✂] capabilities for Synopsys' EDA software;[466]

(b) Project [✂] would not compete with RedHawk/RedHawk-SC as it is not intended to be a signoff software.[467] Project [✂] will enable Synopsys' [✂] and [✂] software ([✂] and [✂]) to perform [✂] analysis to inform [✂], including for multi-die chip designs;[468]

(c) Synopsys lacks the ability and incentive to develop a [✂] signoff software in a sufficiently [✂]. In particular, the Parties submitted that Synopsys had previously entered the market for [✂] with its software product [✂] in [✂]. However, due to [✂] this software product was discontinued from [✂];[469] and

(d) Project [✂] has so far only been tested with a [✂] and the timing of further testing is [✂].[470]

[465] See https://www.ansys.com/products/semiconductors and https://www.solidbasetech.com/ansys/redhawk_sc#:~:text=RedHawk%2C%20the%20industry%20gold%2Dstandard,big%20data%20analytics%20of%20SeaScape.
[466] FMN, paragraph 16.37.
[467] Response to the CMA's Issues Letter paragraph 8.25 dated 27 November 2024.
[468] Synopsys' submission on potential future competition, 8 November 2024, paragraph 2.4.
[469] Parties' additional response to the CMA's Issues Letter, 27 November 2024, paragraph 8.27.
[470] Synopsys' response to the CMA's section 109 Notice, 11 July 2024, Table 2.

*CMA assessment*

293. The CMA considers that the evidence indicates that Project [✂] would not compete with Ansys' RedHawk/RedHawk-SC, regardless of whether it is offered on a [✂] basis or as [✂] capabilities to Synopsys' existing EDA software. In particular, the CMA has seen no evidence of Synopsys benchmarking Project [✂] against [✂] analysis software in its internal documents; indeed, one document notes that a [✂].[471] Synopsys' internal documents support the Parties' submission that the focus of Project [✂] is to [✂] rather than to compete with Ansys.[472] The CMA has seen no evidence to suggest that Project [✂] would be further [✂] into a [✂] signoff software that would compete with Ansys.

294. Further, the CMA notes that, based on the internal documents it has seen, the timing for Project [✂] is [✂], and has undergone only [✂] testing trials with [✂].[473] More generally, based on the evidence the CMA has seen, nothing in Ansys' internal documents indicate that it perceived there to be, or was reacting to the possibility of, any future threat forthcoming from Synopsys in this market.

295. Instead of competing with Project [✂], the CMA considers that the available evidence suggests that Ansys would continue to compete closely with [✂] current gate-level signoff software in the market such as Cadence's Voltus and to a lesser extent, Siemens' mPower. As noted in the Conglomerate effects section, a large number of customers identified Voltus as an alternative to RedHawk/RedHawk-SC, and the majority of these customers identified it as a strong or very strong alternative.[474]

296. Based on the above, the CMA believes that the available evidence does not indicate that the [✂] capabilities being envisaged under Project [✂] would compete with Ansys' RedHawk/RedHawk-SC's signoff product. Ansys' product would also continue to face a strong competitive constraint from Cadence and a more limited constraint from Siemens.

297. Accordingly, the CMA found that the Merger does not give rise to a realistic prospect of an SLC as a result of a loss of future competition in the supply of gate-level power integrity analysis for multi-die chips globally.

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[471] Synopsys' internal documents, Annex SNPSCMA-00012673, '[✂]', January 2024, page 1.
[472] Synopsys' internal documents, Annex Q8(SNPS) – 005, '[✂]', 26 October 2023, slide 23 and 29. Synopsys' internal document, '[✂]', SNPSCMA-00011971, 7 April 2023. Synopsys' internal document, '[✂]', SNPSCMA-00012026, 22 June 2023.
[473] Synopsys' response to the CMA's section 109 Notice, 11 July 2024, Table 2; Synopsys' internal documents, SNPSCMA-00012334, '[✂]', 21 November 2023, page 1. Synopsys' internal document, Annex PN RFI4 – Q16-015 '[✂]', November 2023, slide 11, contained in Annex RFI4Q15(SNPS) – 14, '[✂] RFI 4 – Response Tranche 2', 26 July 2024. With respect to Synopsys' submission that Synopsys lacks the ability and incentive to enter this market, the CMA notes that Synopsys' internal documents indicate that it views this market as a [✂] (Synopsys' internal document, SNPSCMA-00011245, '[✂]', 1 March 2023, slide 7) and that Synopsys may be incentivised to [✂] given the move towards multi-die and Synopsys' capabilities in adjacent or complementary markets. However, for the reasons outlined further in this section, the evidence ultimately does not indicate that Synopsys was seeking to develop a competing product with Project [✂].
[474] Response to the CMA's questionnaire from a number of third parties, November 2024.

### Other theories of harm considered

298. The CMA also considered whether the Parties' overlapping global activities in each of gate-level power consumption analysis, gate-level power integrity, ESD analysis and power device analysis[475] give rise to a realistic prospect of an SLC as a result of horizontal unilateral effects. Based on the evidence reviewed, the CMA believes that the Merger does not give rise to a realistic prospect of an SLC in relation to any of these overlaps and that in each case, the Parties either do not compete at all, or do not compete closely, and the Merged Entity would face sufficient competitive constraints post-Merger. Accordingly, the CMA found that the Merger does not give rise to a realistic prospect of an SLC as a result of horizontal unilateral effects in the global supply of each of gate-level power consumption analysis, gate-level power integrity, ESD analysis and power device analysis for any type of chip.

## COUNTERVAILING FACTORS – ENTRY AND EXPANSION

299. Entry, or expansion of existing firms, can mitigate the initial effect of a merger on competition, and in some cases may mean that there is no SLC. The CMA will consider entry and/or expansion plans of rivals who do so in direct response to the merger as a countervailing measure that could prevent an SLC. In assessing whether entry or expansion might prevent an SLC, the CMA considers whether such entry or expansion would be timely, likely and sufficient.[476]

300. The Parties submitted that there have been a number of new entrants into EDA, optics and photonics software in recent years. They pointed, in particular, to a number of Chinese new entrants benefiting from significant government investment, as well as a number of Chinese suppliers that have been present in EDA markets for more than five years receiving investor interest.[477] The Parties also listed a number of non-Chinese entrants, as well as the availability of open-source EDA tools.[478]

301. As a starting point, as set out above, for the CMA to consider entry and expansion as a countervailing factor, it would need to occur as a result of the Merger.[479] Entry or expansion that would occur irrespective of the Merger is considered above in the theories of harm. The CMA has not seen any evidence of entry or expansion being planned or occurring as a response to the Merger.

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[475] In terms of use cases, gate-level power consumption analysis is used at a later design stage (in comparison to RTL power consumption analysis, which is used at an early design stage) to check how much power a digital chip consumes (FMN, paragraph 14.118); gate-level power integrity analysis checks a digital chip's reliability when using power, to ensure it will function correctly (FMN, paragraph 14.129); ESD analysis tests for chip failure from the unwanted transfer of static electricity (FMN, paragraph 14.136) and power device analysis checks the efficiency and reliability of power devices at the physical verification and signoff stage of analog and custom chip designs (FMN, paragraph 14.168).
[476] CMA129, paragraph 8.31.
[477] FMN paragraphs 22.1, 22.2, 22.7.
[478] FMN paragraphs 22.4-22.6.
[479] CMA129, paragraph 8.28.

302. Evidence from the Parties' internal documents and from third parties indicates that barriers to entry and expansion are high, in particular because of the high levels of R&D investment, technical expertise and time required to develop EDA, S&A, optics and photonics software. For example, one Synopsys internal document refers to challenges in photonic chip design development due to the [✂] of photonic experts.[480] As included in paragraphs 122 and 134 above, third parties noted the significant time and cost required to enter optics or photonics software. The CMA believes that entry or expansion would not be sufficient to prevent a realistic prospect of an SLC as a result of the Merger.

## CONCLUSION ON SUBSTANTIAL LESSENING OF COMPETITION

303. Based on the evidence set out above, the CMA believes that it is or may be the case that the Merger may be expected to result in an SLC as a result of horizontal unilateral effects in relation to the supply of RTL power consumption analysis for digital chips globally, optics software globally, and photonics software globally.

[480] Synopsys Internal Document, Annex Q10(SNPS) - 042 – '[✂]', August 2023, page 7.

# DECISION

304. Consequently, the CMA believes that it is or may be the case that (i) arrangements are in progress or in contemplation which, if carried into effect, will result in the creation of a relevant merger situation; and (ii) the creation of that situation may be expected to result in an SLC within a market or markets in the United Kingdom.

305. The CMA therefore believes that it is under a duty to refer under section 33(1) of the Act. However, the duty to refer is not exercised whilst the CMA is considering whether to accept undertakings under section 73 of the Act instead of making such a reference.[481] The Parties have until 31 December 2024[482] to offer an undertaking to the CMA.[483] The CMA will refer the Merger for a phase 2 investigation[484] if the Parties do not offer an undertaking by this date; if the Parties indicate before this date that they do not wish to offer an undertaking; or if the CMA decides[485] by 8 January 2025 that there are no reasonable grounds for believing that it might accept the undertaking offered by the Parties, or a modified version of it.

**Naomi Burgoyne**
**Senior Director, Mergers**
**Competition and Markets Authority**
**20 December 2024**

[481] Section 33(3)(b) of the Act.
[482] Section 73A(1) of the Act.
[483] Section 73(2) of the Act.
[484] Sections 33(1) and 34ZA(2) of the Act.
[485] Section 73A(2) of the Act.