CLAIM NO. HP-2020-000017

IN THE HIGH COURT OF JUSTICE
BUSINESS AND PROPERTY COURTS OF ENGLAND AND WALES
INTELLECTUAL PROPERTY LIST (ChD)
PATENTS COURT

B E T W E E N:

COMMSCOPE TECHNOLOGIES LLC
(incorporated under the laws of the state of Delaware, USA)

Claimant

- and –

SOLiD Technologies, Inc.
(a UK establishment of SOLiD, Inc., a company incorporated under the laws of South Korea)

Defendant

STATEMENT OF REASONS FOR AMENDMENT OF EP(UK) 2 290 850 B1

The following are the reasons in support of the application by the Claimant to amend European Patent No EP(UK) 2 290 850 B1 ("**EP 850**").

1. The Claimant will contend that the claims of EP 850 as granted are valid. However, if they are held to be invalid, the Claimant will seek conditionally to amend the claims of EP 850 as shown in Annex A hereto. The amendments are sought to limit the invention, and meet the objection to the validity of EP 850 by anticipation and/or obviousness over the prior art reference "Oh" raised by the Defendant in its Grounds of Invalidity dated 26 August 2020.

2. The amendment to claim 1 of EP 850 is supported by page 12 of WO 2002/09319 A1, where it states, "*The digitized signals output at each demultiplexer 441-1 to 441-P are then applied to FPGA 467 where the signals are summed together*". The "FPGA" is a Field Programmable Gate Array which receives digitized signals. The summing of signals is shown in Figure 4 at block 498, which is inside the FPGA 467. The amendment is further supported by page 7 where it states, "*Both DHU 20 and DEU 30 split signals in the forward path and sum signals in the reverse path. In order to accurately sum the digital signals together at DHU 20 or DEU 30 the data needs to come in to the DHU 20 or DEU 30 at exactly the same rate. As a result all of the DRUs 40 and 40' need to be synchronized so that their digital sample rates are all locked together. Synchronizing the signals in time is accomplished by locking everything to the bit rate over the fiber".*

3. The amendment to claim 7 of EP 850 is supported by page 16 of WO 2002/09319 A1, where it states, "*In one embodiment, the FPGA 661 includes summer 665 which mathematically sums together the digital RF signals received from demultiplexers 671-1 to 671-X* " and Figure 6 where the "Overflow Handling Algorithm" is depicted.

4. The amendment to claim 8 of EP 850 is supported by page 13 of WO 2002/09319 A1, where it states, *"… in one embodiment each of the digital RF signals received from fibers 416-1 to 416-P, where P is equal to 6, comprise 14 bit inputs. All of those 6 different 14 bit inputs then go into summer 498. In order to allow for overflow, at least 17 bits of resolution is needed in the summer 498 to handle a worst-case scenario when all 6 of the 14 bit inputs are at full scale at the same time. In this embodiment, a 17-bit wide summer 498 is employed to handle that dynamic range. Coming out of summer 498 is needed a 14-bit signal going in the reverse path."* and *"In an alternate embodiment, overflow algorithm circuit 496 controls the gain and scales the signal dynamically to handle overflow conditions"*, and Figure 4, which shows the "Overflow Algorithm" at block

496 inside the FPGA 467.

5. The amendment to claim 9 is supported by page 7 of WO 2002/09319 A1, where it states, "*Both DHU 20 and DEU 30 split signals in the forward path and sum signals in the reverse path. In order to accurately sum the digital signals together at DHU 20 or DEU 30 the data needs to come in to the DHU 20 or DEU 30 at exactly the same rate. As a result all of the DRUs 40 and 40' need to be synchronized so that their digital sample rates are all locked together. Synchronizing the signals in time is accomplished by locking everything to the bit rate over the fiber".*

6. As described in paragraphs 2 to 5 above, the amendments sought will not have the effect of disclosing any matter which extends beyond that disclosed in the application as filed or of extending the protection conferredby EP 850. The amendments therefore comply with the provisions of the Patents Act 1977 and in particular sections 75 and 76 thereof.

7. There are no reasons why the amendments should not be allowed.

Statement of Truth

The Claimant believes that the facts stated in this Statement of Reasons are true. I am duly authorised by the Claimant to sign this statement. I understand that proceedings for contempt of court may be brought against anyone who makes, or causes to be made, a false statement in a document verified by a statement of truth without an honest belief in its truth.

Signed:  Date: 1 September 2021

Served this 1st day of September 2021 by Powell Gilbert LLP, 85 Fleet Street, London EC4Y 1AE (Ref: CMM13.1/APL/TW), Solicitors for the Claimant.

Annex A

1. A digital host unit (20, 420) to communicatively couple to a plurality of digital remote units (40, 540), the digital host unit (20, 420) comprising a radio frequency interface to receive an original forward-path analog radio frequency signal from a wireless interface device (10, 211, 310) and to communicate a reverse-path analog radio frequency signal to the wireless interface device (10, 211, 310), wherein each of the plurality of digital remote units (40, 540) receives a respective original reverse-path analog radio frequency signal comprising a reverse-path radio frequency spectrum and wherein each of the plurality of digital remote units (40, 540) generates respective reverse-path digital samples indicative of the respective original reverse-path analog radio frequency signal received at that digital remote unit;

and characterized in that the digital host unit (20, 420) comprises:

an analog-to-digital converter (464) to convert the original forward-path analog radio frequency signal to forward-path digital samples;

at least one transmission line interface (431-1, 431-2, 431-P, 418-1, 418-2, 418-P) to communicate the forward-path digital samples to at least one of the plurality of digital remote units (40, 540) and to receive the reverse-path digital samples from the plurality of digital remote units (40, 540);

a digital summer (498) to digitally sum corresponding reverse-path digital samples received from the plurality of digital remote units (40, 540) to produce summed reverse-path digital samples; ~~and~~

a digital-to-analog converter (494) to convert the summed reverse-path digital samples to a reconstructed reverse-path analog radio frequency signal;

a field programmable gate array (FPGA) (467) which comprises the digital summer (498); and

a means to communicate to each of the plurality of digital remote units (40, 540) a signal to enable each of the plurality of digital remote units (40, 540) to synchronise their digital sample rate to that signal.

2. The digital host unit (20, 420) of claim 1, wherein each of the at least one of the plurality of digital remote units (40, 540) to which the digital host unit (20, 420) communicates the digital

samples converts the forward-path digital samples to a reconstructed forward-path analog radio frequency signal.

3. The digital host unit (20, 420) of claim 1, wherein the digital host unit (20, 420) comprises a multiplexer (466) to frame the forward-path digital samples for communication to the plurality of digital remote units (40, 540) as a forward-path framed serial bit stream.

4. The digital host unit (20, 420) of claim 1, wherein each of the plurality of digital remote units (40, 540) multiplexes the respective reverse-path digital samples for communication to the digital host unit (20, 420) as a respective reverse-path multiplexed signal; and

wherein the digital host unit (20, 420) comprises at least one demultiplexer (441) to extract the respective reverse-path digital samples from the respective reverse-path multiplexed signals received from the plurality of digital remote units (40, 540).

5. The digital host unit (20, 420) of claim 1, wherein the digital host unit (20, 420) communicates the reconstructed reverse-path analog radio frequency signal to at least one base station and, optionally, wherein the reconstructed reverse-path analog radio frequency signal is communicated from the digital host unit (20, 420) to the at least one base station using at least one bi-directional amplifier (211).

6. The digital host unit (20, 420) of claim 1, wherein the digital summer (498) digitally sums the corresponding reverse-path digital samples received from the plurality of digital remote units (40, 540) at a resolution greater than a resolution of the reverse-path digital samples being summed.

7. The digital host unit (20, 420) of claim 1, wherein a second plurality of digital remote units (40') are communicatively coupled to the digital host unit (20, 420) using a digital expansion unit (30, 630) that is communicatively coupled to the digital host unit (20, 420);

wherein each of the second plurality of digital remote units (40') receives a respective original reverse-path analog radio frequency signal comprising the reverse-path radio frequency spectrum;

wherein each of the second plurality of digital remote units (40') generates respective reverse-path digital samples indicative of the respective original reverse-path analog radio frequency signal received at that digital remote unit (40');

wherein each of the second plurality of digital remote units (40') communicates the respective reverse-path digital samples generated by that digital remote unit (40') to the digital expansion unit (30, 630);

wherein the digital expansion unit (30, 630) digitally sums corresponding reverse-path digital samples received from the second plurality of digital remote units (40') to produce summed reverse-path digital samples;

wherein the digital expansion unit (30, 630) communicates the summed reverse-path digital samples to the digital host unit (20, 420); and

wherein the digital host unit (20, 420) digitally sums the reverse-path digital samples received from the digital expansion unit (30, 630) with corresponding digital samples received from the plurality of digital remote units (40, 540);

and wherein the digital expansion unit (3, 630) comprises a field programmable gate array (FPGA) (661) which comprises the digital summer (665).

8. The digital host unit (20, 420) of claim 1, wherein the digital-to-analog converter (494) has an associated input bit-resolution and wherein the digital host unit (20, 420) comprises an overflow algorithm circuit (496) that is configured to keep the summed reverse-path digital samples within the input bit resolution associated with the digital-to-analog converter (494) by controlling the gain and scaling the signal dynamically to handle overflow conditions.

9. A method of distributing radio frequency signals using a digital host unit (20, 420) and a plurality of digital remote units (40, 540), the method comprising:

receiving, at the digital host unit (20, 420), an original forward-path analog radio frequency signal from a wireless interface device (10, 211, 310);

receiving, at each of the plurality of digital remote units (40, 540), a respective original reverse-path analog radio frequency signal comprising a reverse-path radio frequency spectrum;

generating, at each of the plurality of digital remote units (40, 540), respective reverse-path digital samples indicative of the respective original reverse-path analog radio frequency signal received at that digital remote unit; and

communicating, at each of the plurality of digital remote units (40, 540), the respective reverse-path digital samples generated by that digital remote unit to the digital host unit (20, 420) across a transmission line (216, 316);

and characterized by:

converting, at the digital host unit (20, 420), the original forward-path analog radio frequency signal to forward-path digital samples;

communicating the forward-path digital samples to at least one of the plurality of digital remote units (40, 540) across at least one transmission line (214, 314);

digitally summing, at the digital host unit (20, 420), corresponding reverse-path digital samples received from the plurality of digital remote units (40, 540) to produce summed reverse-path digital samples; and

converting, at the digital host unit (20, 420), the summed reverse-path digital samples to a reconstructed reverse-path analog wireless radio frequency signal;

and wherein the digital host unit (20, 240) communicates to each of the plurality of digital remote units (40, 540) a signal to enable each the digital remote units (40, 540) to synchronise their digital sample rate to that signal;

and wherein each of the digital remote units (40, 540) synchronise their digital sample rate to the signal of the digital remote unit (40, 540).

10. The method of claim 9, wherein each of the plurality of digital remote units (40, 540) multiplexes the respective reverse-path digital samples for communication to the digital expansion unit as a respective reverse-path multiplexed signal;

wherein the method further comprises, at the digital host unit (20, 420), for each of the plurality of digital remote units (40, 540), extracting the respective reverse-path digital samples from the respective reverse-path multiplexed signal received from that digital remote unit.

11. The method of claim 9, wherein the corresponding reverse-path digital samples are digitally summed at a resolution greater than a resolution of the reverse-path digital samples being summed.

12. The method of claim 9, wherein converting, at the digital host unit (20, 420), the summed reverse-path digital samples to the reconstructed reverse-path analog wireless radio frequency signal comprises converting, at the digital host unit (20, 420) the summed reverse-path digital samples to the reconstructed reverse-path analog wireless radio frequency signal using an associated input bit resolution; and

wherein the method further comprises keeping the bit resolution of the summed reverse-path digital samples within the associated input bit resolution.

13. The method of claim 9, wherein at least one digital remote unit (40') is communicatively coupled to the digital host unit (20, 420) using at least one digital expansion unit (30, 630).

14. The digital host unit (20, 420) of claim 1, wherein the at least one transmission line interface (431-1, 431-2, 431-P, 418-1, 418-2, 418-P) includes at least one optical transmitter (431-1, 431-2, 431-P, 418-1, 418-2, 418-P).

15. The method of claim 9, wherein the at least one transmission line (214,314) includes at least one optical fiber (214, 314).