EP 1163622 – proposed amended claims

1. A signal interface circuit for providing an interface between a simulation system and a system under test comprising circuit portions operable to provide a digital interface, and circuit portions operable to provide an analogue interface, the circuit further comprising control means operable selectively to enable or disable the said circuit portions, so as to reconfigure the interface provided by the signal interface circuit, in which the circuit further comprises a load connectable between a terminal on which an input signal is received, and a power rail, whereby to apply a loading to the input signal.

2. A signal interface circuit according to claim 1 in which the circuit portions are individually selectable to configure the circuit as a digital or analogue device.

3. A signal interface circuit according to claim 1 or 2 in which the circuit comprises circuit portions operable to provide an input interface and circuit portions operable to provide an output interface.

4. A signal interface circuit according to any preceding claim in which the circuit comprises a plurality of switch means operable to reconfigure the interface by connecting and disconnecting corresponding circuit portions.

5. A signal interface circuit according to claim 4 in which the switch means comprise analogue switches.

6. A signal interface circuit according to claim 4 or 5 in which the state of the switch means is determined by data supplied by the control means.

7. A signal interface circuit according to claim 6 in which the data is binary data which sets the state of the switch means.

8. A signal interface circuit according to claim 6 or 7 in which the control means comprises storage means storing data bits which set the state of the switch means.

9. A signal interface circuit according to claim 8 in which the storage means comprises a shift register.

10. A signal interface circuit according to claim 8 or 9 in which the control means comprises a data input port operable to receive control data for storage in the storage means.

11. A signal interface circuit according to claim 10 in which the data input port is a serial data port.

12. A signal interface circuit according to any preceding claim in which the circuit forms part of an array of like circuits, each providing a respective interface channel.

13. A signal interface circuit according to claim 12 and any of claims 8 to 11, wherein the storage means of the circuits are connected in series to allow control data to be passed from circuit to circuit.

14. A signal interface circuit according to claim 12 and any of claims 8 to 11, wherein the storage means of the circuits are connected in parallel to allow control data to be passed from circuit to circuit.

15. A signal interface circuit according to any of claims 3 to 14 in which the circuit comprises circuit portions operable to provide a digital input interface.

16. A signal interface circuit according to claim 15 in which the digital input interface includes a threshold detector.

17. A signal interface circuit according to claim 16 in which the digital input interface additionally incorporates a buffer circuit, a ~~fitter~~ filter circuit or a variable gain amplifier.

18. A signal interface circuit according to any of claims 3 to 17 in which the circuit comprises circuit portions operable to provide an analogue input interface.

19. A signal interface circuit according to claim 18 in which the analogue input interface comprises a buffer amplifier.

20. A signal interface circuit according to claim 19 in which the analogue input interface additionally incorporates a variable gain amplifier or a filter circuit.

21. [Claim deleted] ~~A signal interface circuit according to any preceding claim in which the circuit further comprises a load connectable between a terminal on which an input signal is received, and a power rail.~~

22. A signal interface circuit according to any preceding claim ~~21~~ in which the load is connectable selectively to a high or low power rail ~~whereby to apply a loading to the input signal~~.

22A. A signal interface circuit according to any preceding claim in which the load is connectable at one side to the terminal and at the other side to a switch to connect the load to ground or to a positive rail, according to the state of the switch, and in which the setting of the switch is determined by the control means.

22B. A signal interface circuit according to any preceding claim in which the impedance of the load is variable and in which the degree of loading is set by the setting of the load.

22C. A signal interface circuit according to claim 22B in which the circuit can output a signal which is either held hard to logic high, or allowed to decay at a rate controlled by the setting of the load.

22D. A signal interface circuit according to claim 22B or 22C in which the load is a variable resistance.

22E. A signal interface circuit according to any preceding claim in which the circuit is configured to receive a signal and, in accordance with a digital state of that signal, output a logic high level or a logic low level, the logic high and the logic low levels being set independently of the logic levels of that signal and of each other.

22F. A signal interface circuit according to claim 22E in which the control means is configured to set the logic high and logic low levels.

23. A signal interface circuit according to any preceding claim ~~22~~ in which the voltage of the power rail is selectively configurable to be at one of a plurality of predetermined voltage levels.

24. A signal interface circuit according to claim 23 in which the power rail is configurable in response to data received from the control means.

25. A signal interface circuit according to any of claims 3 to 24 in which the circuit comprises circuit portions operable to provide a digital output interface to an output terminal.

26. A signal interface circuit according to claim 25 when dependent on any of claims 3 to 22, 23 or 24 in which the circuit portions comprise two switches connected between the output terminal and, respectively, low and high logic levels, the switches being closable to pull the output terminal to the corresponding logic level, the switch to be closed being selected in accordance with the logic level of a signal received.

27. A signal interface circuit according to claim 26 in which the circuit portions further comprise a load connectable between the output terminal and, selectively, the low and high logic levels, to load the output terminal.

28. A signal interface circuit according to claim 26 or 27 in which operation of the switches is selectively disabled by the control means, whereby the output is either pulled to a selected logic level or loaded by the load.

29. A signal interface circuit according to any of claims 3 to 28 in which the circuit comprises circuit portions operable to provide an analogue output interface.

30. A signal interface circuit according to claim 29 in which the analogue output interface incorporates an amplifier, such as a buffer amplifier.

31. A signal interface circuit according to claim 30 in which the analogue output interface additionally incorporates a variable gain amplifier and/or a filter circuit.

32. A multi-channel signal interface system comprising a plurality of signal interface circuits ~~according to any preceding claim~~,
each such signal interface circuit comprising circuit portions operable to provide a digital interface, and circuit portions operable to provide an analogue interface,
each such circuit further comprising control means operable selectively to enable or disable the said circuit portions, so as to reconfigure the interface provided by the signal interface circuit,
in which each such circuit further comprises a load connectable between a terminal on which an input signal is received, and a power rail, whereby to apply a loading to the input signal,
each such circuit providing an interface between a simulation system and a system under test, the simulation system being operable to provide signals in accordance with a simulation being conducted and to receive signals indicative of the response of the system under test, the signals being provided and received through the interface circuits, and the interface circuits being individually reconfigurable as aforesaid.

33. A multi-channel signal interface system according to claim 32 in which each such signal interface circuit further comprises the features of any of claims 2 to 31.