

selection logic configured to select one of the logic chains in dependence on the input variable so as to provide, for the received input variable, an approximate value of the mathematical function.

Each of the fixed gradients in the predetermined set of fixed gradients has a minimum Hamming weight, h , which is less than or equal to a threshold value, wherein the threshold value determines a limit on the number of adders that the binary multiplier is adapted to use for performing a multiplication.

The threshold value may be 2 or 3.

The minimum Hamming weight h may be less than or equal to 3.

The selection logic may be configured to select one of the logic chains by comparing the received input variable to a predetermined set of break values, each break value representing a value of the input variable delimiting one or more linear segments.

The selection logic may be configured to determine a pair of adjacent break values between which the received input variable lies and, responsive to that determination, select the logic chain corresponding to the linear segment lying between that pair of adjacent break values.

~~Each of the set of break values may be used in the selection logic in the form of:~~

~~a binary representation of the break value;~~

~~a trinary representation of the break value; or~~

~~a representation of the break value as a product of two binary numbers, two trinary numbers, or a binary and a trinary number;~~
~~the form used for each break value being the representation of that break value having the minimum Hamming weight.~~

~~The minimum Hamming weight of each of the set of break values may be less than or equal to 3.~~

CLAIMS

1. A binary logic circuit for approximating a mathematical function over a predefined range as a series of linear segments, each linear segment having one of a predetermined set of fixed gradients and a corresponding base value, the binary logic circuit comprising:
 - an input for receiving an input variable in the predefined range;
 - a plurality of logic chains each comprising:
 - a binary multiplier adapted to perform multiplication by a respective one of the set of fixed gradients using $h-1$ binary adders, where h is the minimum Hamming weight of:
 - a binary representation of the fixed gradient;
 - a trinary representation of the fixed gradient; and
 - a representation of the fixed gradient as a product of two binary numbers, two trinary numbers, or a binary and a trinary number;
 - the $h-1$ binary adders being logically configured to perform the multiplication using the representation of the fixed gradient having that minimum Hamming weight h ; and
 - a binary adder adapted to add a base value to the input or output of the binary multiplier; and
 - selection logic configured to select one of the logic chains in dependence on the input variable so as to provide, for the received input variable, an approximate value of the mathematical function,
 - wherein each of the fixed gradients in the predetermined set of fixed gradients has a respective minimum Hamming weight, h , which is less than or equal to a threshold value, wherein the threshold value determines a limit on the number of adders that the binary multiplier is adapted to use for performing a multiplication.
2. A binary logic circuit as claimed in claim 1, wherein the threshold value is 2 or 3.
3. A binary logic circuit as claimed in claim 1, wherein the minimum Hamming weight h is less than or equal to 3.

4. A binary logic circuit as claimed in any preceding claim, the selection logic being configured to select one of the logic chains by comparing the received input variable to a predetermined set of break values, each break value representing a value of the input variable delimiting one or more linear segments.

5. A binary logic circuit as claimed in claim 4, the selection logic being configured to determine a pair of adjacent break values between which the received input variable lies and, responsive to that determination, select the logic chain corresponding to the linear segment lying between that pair of adjacent break values.

~~6. A binary logic circuit as claimed in claim 4 or 5, wherein each of the set of break values is used in the selection logic in the form of:~~

~~a binary representation of the break value;~~

~~a trinary representation of the break value; or~~

~~a representation of the break value as a product of two binary numbers, two trinary numbers, or a binary and a trinary number;~~

~~the form used for each break value being the representation of that break value having the minimum Hamming weight.~~

~~7. A binary logic circuit as claimed in claim 6, wherein the minimum Hamming weight of each of the set of break values is less than or equal to 3.~~

68. A binary logic circuit as claimed in any preceding claim, wherein the mathematical function is expressed in the form $y = f(x)$, where x and y represent values along respective Cartesian axes.

79. A binary logic circuit as claimed in claim 68, the binary adder of each logic chain being arranged to add the respective base value to the output of the binary multiplier.

840. A binary logic circuit as claimed in claim 79, wherein each linear segment represents part of a line that crosses the y axis at the base value.

| 914. A binary logic circuit as claimed in claim 68, the binary adder of each logic chain being arranged to add the respective base value to the received input variable.

| 1042. A binary logic circuit as claimed in claim 944, wherein each linear segment represents part of a line that crosses the x axis at the base value.

| 1143. A binary logic circuit as claimed in any preceding claim, the plurality of binary multipliers comprising at least three binary multipliers.

| 1244. A binary logic circuit as claimed in any preceding claim, wherein the mathematical function is a continuous smooth function over the predefined range.

| 1346. A binary logic circuit as claimed in any preceding claim, wherein the mathematical function is a base 2 logarithm and the predefined range is between 1 and 2.

| 1446. A binary logic circuit as claimed in any of claims 1 to 1244, wherein the mathematical function is a gamma function and the predefined range is between 0 and 1.

| 1547. A binary logic circuit as claimed in any preceding claim, wherein at least one of the plurality of logic chains comprises a binary multiplier adapted to perform multiplication by a fixed gradient having a minimum hamming weight of greater than one.

| 1648. A machine readable storage medium having encoded thereon non-transitory machine readable code for generating a binary logic circuit according to any of claims 1 to 17.

| 1749. A method of deriving a hardware representation of a binary logic circuit configured to approximate a mathematical function over a predefined range as a series of linear segments, the method comprising:

fitting a plurality of linear segments to the function over the predefined range, each segment extending between a pair of break points and having a fixed gradient selected from a predetermined set of fixed gradients,

determining a base value for each of the segments; and

deriving a hardware representation for a binary logic circuit which comprises:

for each of the plurality of linear segments:

a binary multiplier adapted to perform multiplication by the selected fixed gradient of the segment using $h-1$ binary adders, where h is the minimum Hamming weight of:

a binary representation of the fixed gradient;

a trinary representation of the fixed gradient; and

a representation of the fixed gradient as a product of two binary numbers, two trinary numbers, or a binary and a trinary number;

wherein the $h-1$ binary adders are logically configured to perform multiplication using the representation of the fixed gradient having the minimum Hamming weight h ; and

a binary adder adapted to add the determined base value to the input or output of the binary multiplier;

and

selection logic adapted to select, for a given input variable in the predefined range, one of the plurality of binary multipliers in dependence on the determined break points,

wherein each of the fixed gradients in the predetermined set of fixed gradients has a minimum Hamming weight, h , which is less than or equal to a threshold value, wherein the threshold value determines a limit on the number of adders that the binary multiplier is adapted to use for performing a multiplication.

1820. The method of claim 1749, wherein the threshold value is 2 or 3.

1924. A method as claimed in claim 1749, wherein the minimum Hamming weight h is less than or equal to 3.

2022. A method as claimed in any of claims 17 to 19 to 21, further comprising:

for each of the plurality of linear segments, calculating an average gradient between the break points delineating that linear segment; and

selecting the closest fixed gradient to the calculated average gradient from the predetermined set of fixed gradients, the set of fixed gradients comprising gradients which are represented as binary representations, trinary representations and representations being the product of two binary numbers, two trinary numbers, or a binary and a trinary number.

2123. A method as claimed in any of claims 17 to 2019 to 22, further comprising selecting a sufficient number of the plurality of linear segments such that the binary logic circuit achieves at least a predetermined accuracy substantially over the predefined range of values for the input variable.

2224. A method as claimed in any of claims 17 to 2119 to 23, wherein the hardware representation is RTL, a hardware description language, or a gate-level description language.

2325. A method as claimed in claim 2224, wherein the hardware description language is Verilog or VHDL.

2426. A method as claimed in claim 2224, wherein the gate-level description language is OASIS or GDSII.

2527. A computer readable storage medium having encoded thereon non-transitory computer readable program code for generating a hardware representation according to the method of any of claims 17 to 2419 to 26.

2628. A data processing device configured for generating a hardware representation according to the method of any of claims 17 to 2419 to 26.

2729. A method of manufacturing a binary logic circuit in accordance with a hardware representation derived using the method of any of claims 17 to 24~~19 to 26~~.