FIG1

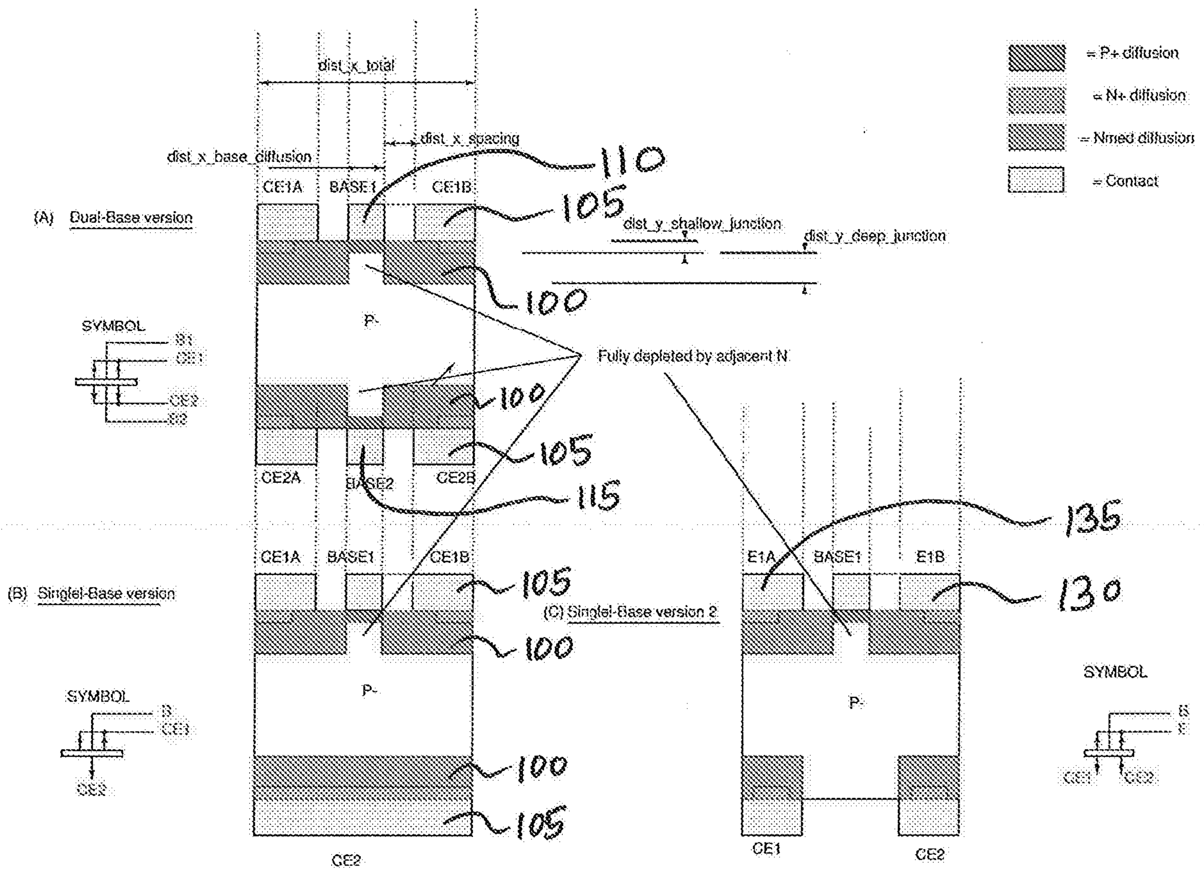


FIG2a - Test Circuit

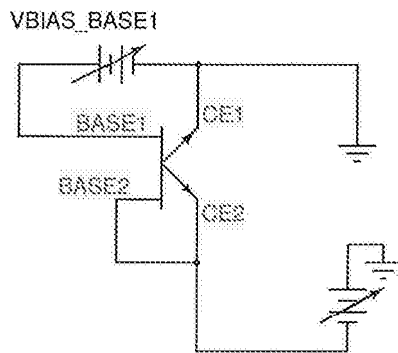


Fig2c Power scavenging concept

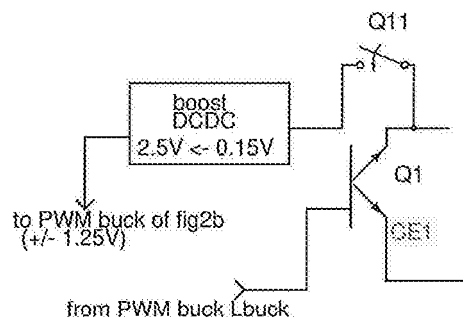
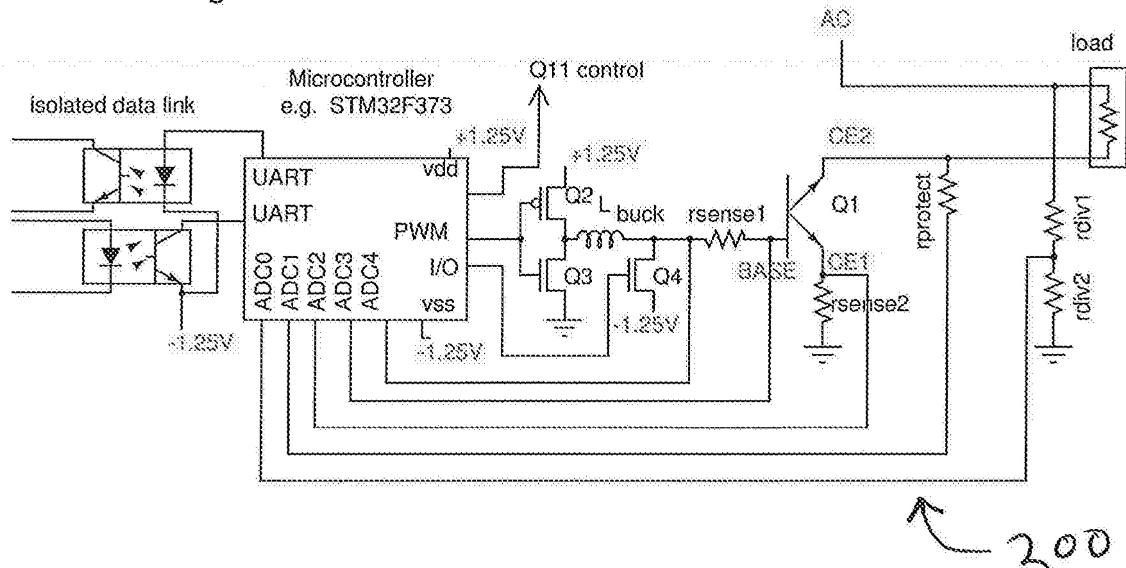


FIG2b - Intelligent Drive circuit



200

Fig 3a, Hole current density at 0.6V Vbe - top base driven only

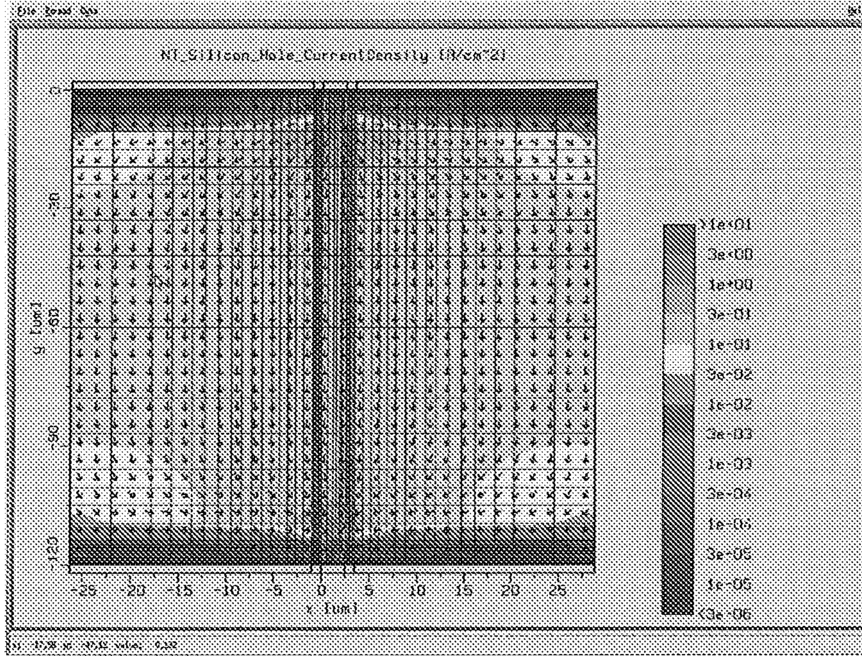


Fig 3b, Electron current density at 0.6V Vbe - top base driven only

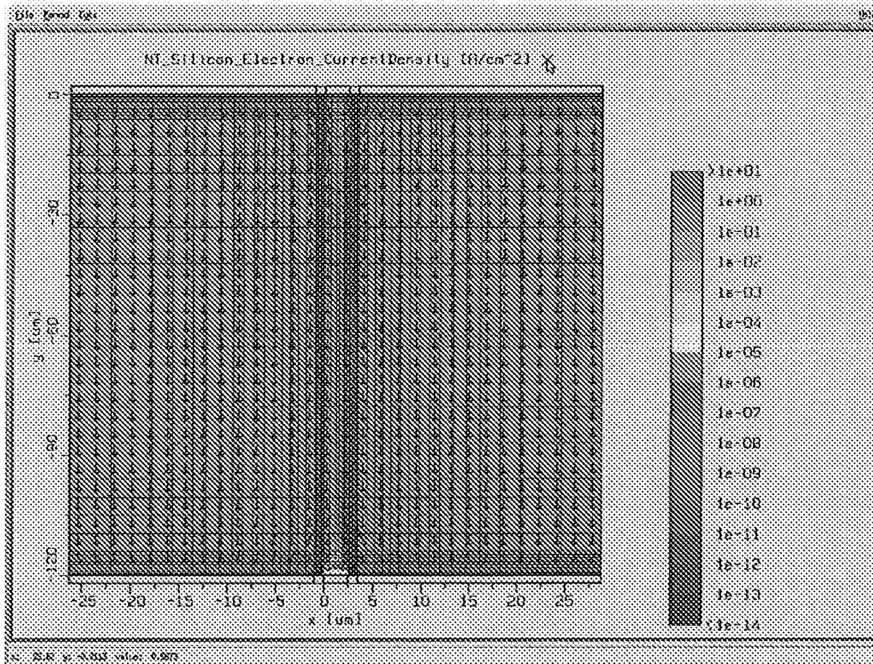
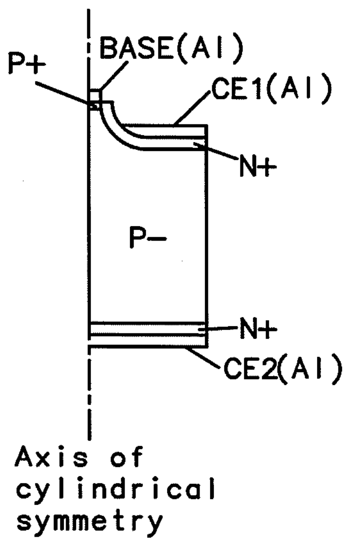


Fig4a



Al = aluminium

Fig4b

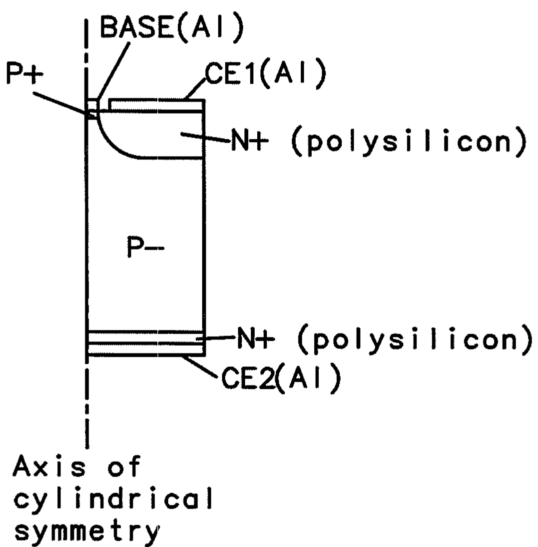


Fig4c

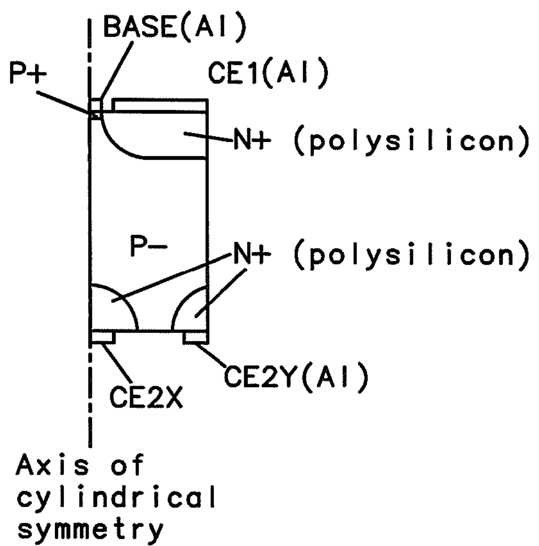
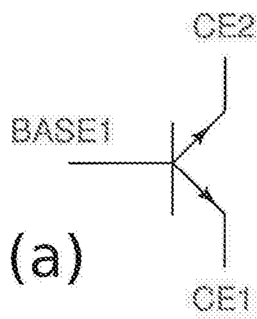


FIG5

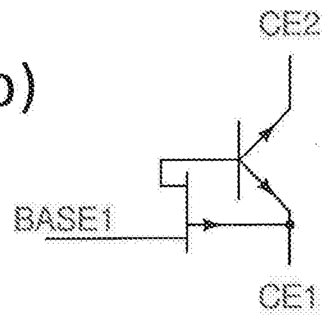
SYMBOL

EQUIVALENT CIRCUIT



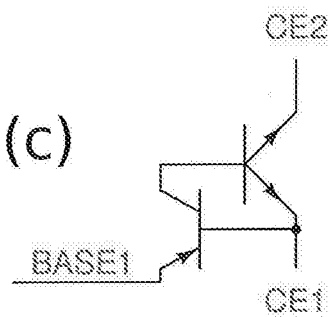
(a)

(b)



non-encroachment of donors in channel

(c)



encroachment of donors in channel

FIG6

Additional circuits for power scavenging

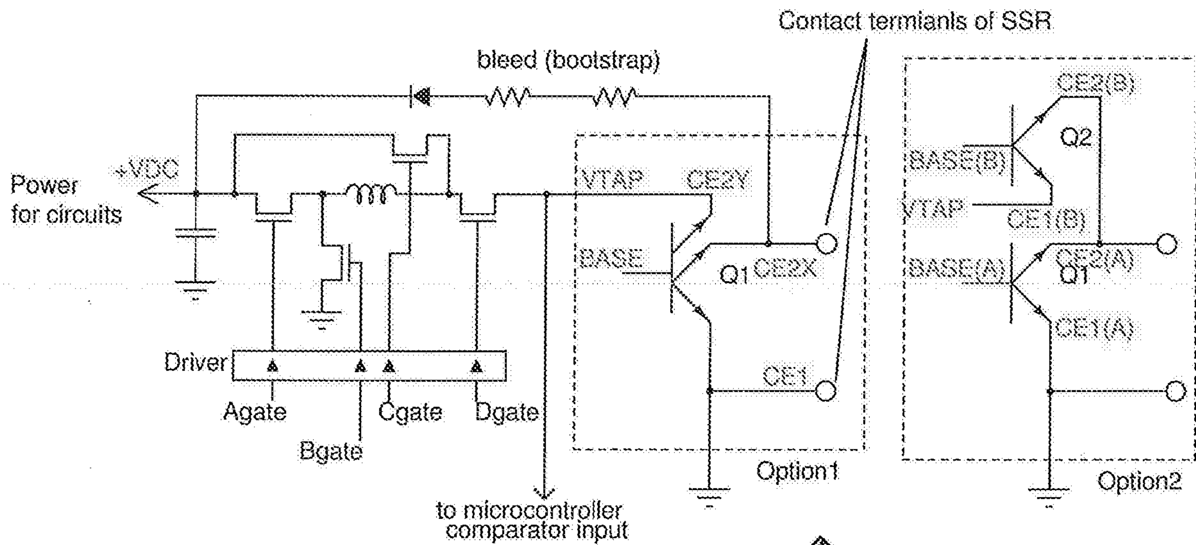


Fig 7

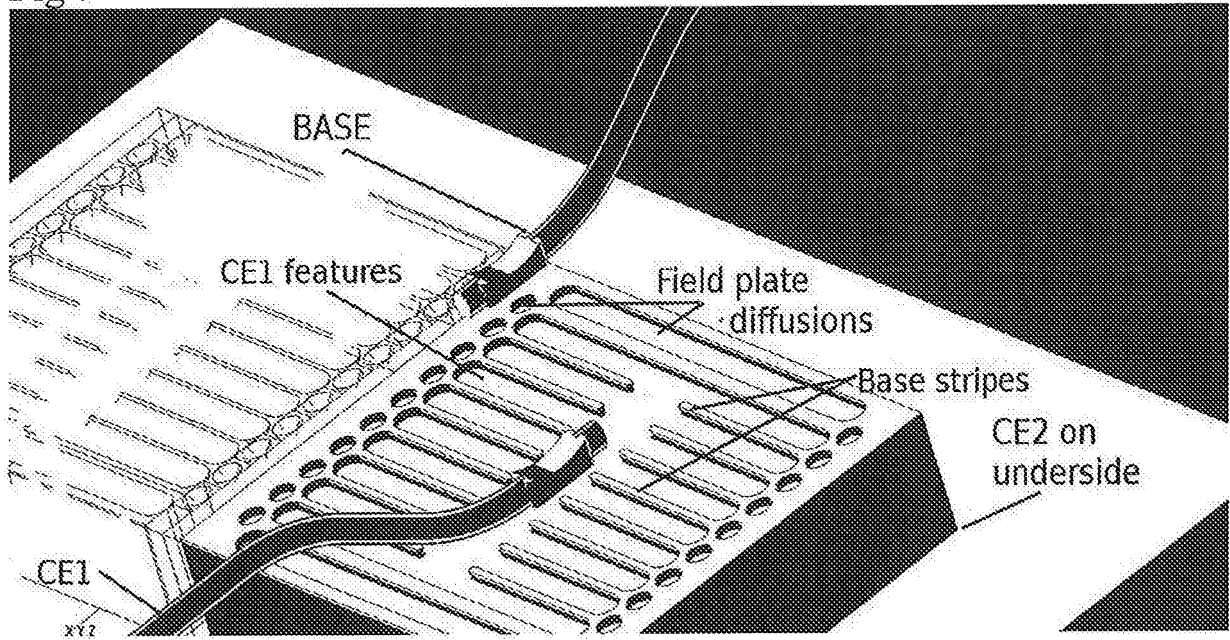


Fig8

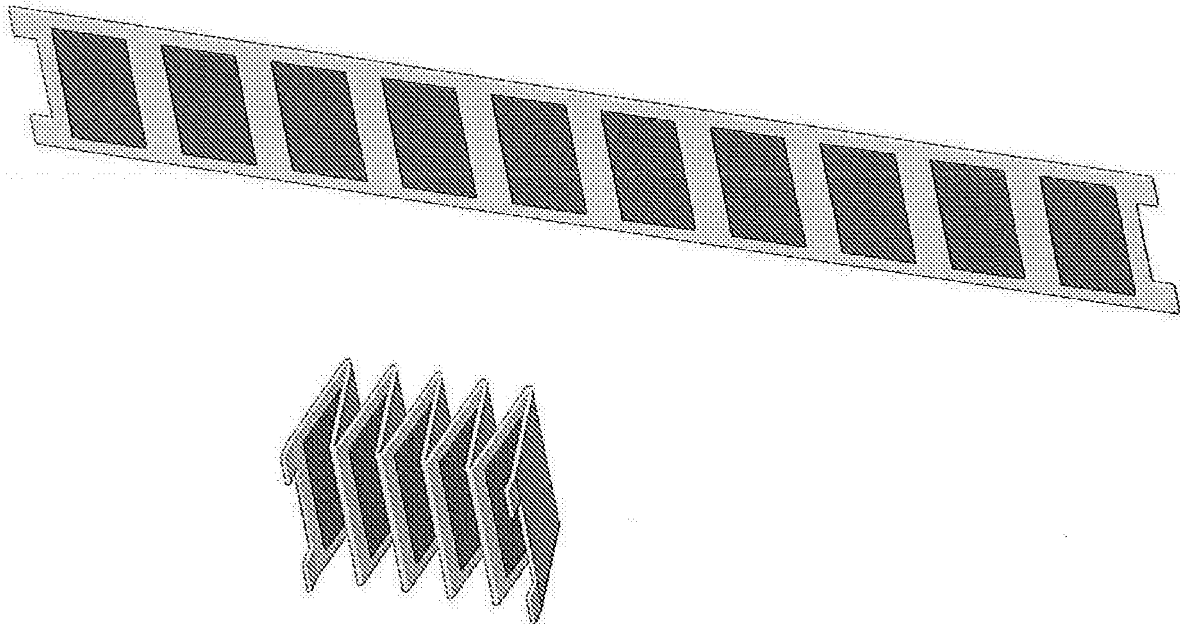


Fig 9

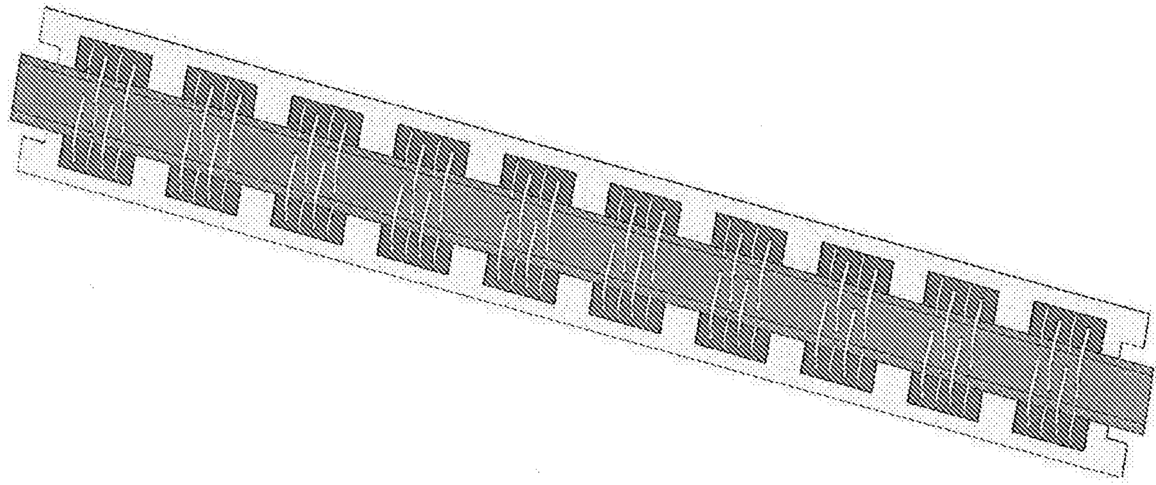
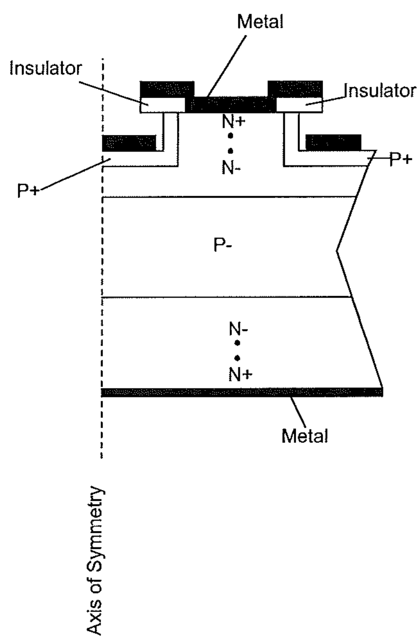
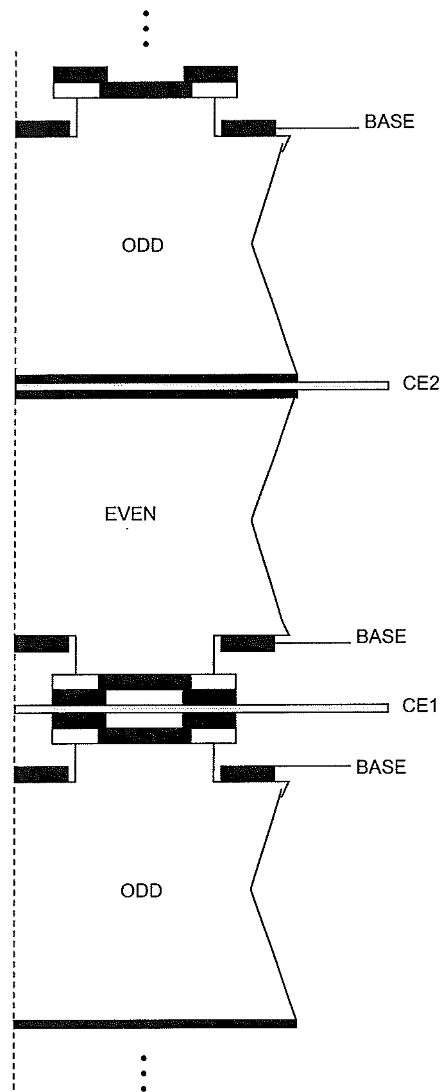


FIG10. Recessed 'BASE' PNP base version



(a) Unit design. Cylindrical symmetry



(b) Stacked design for higher current or higher voltage

Fig11

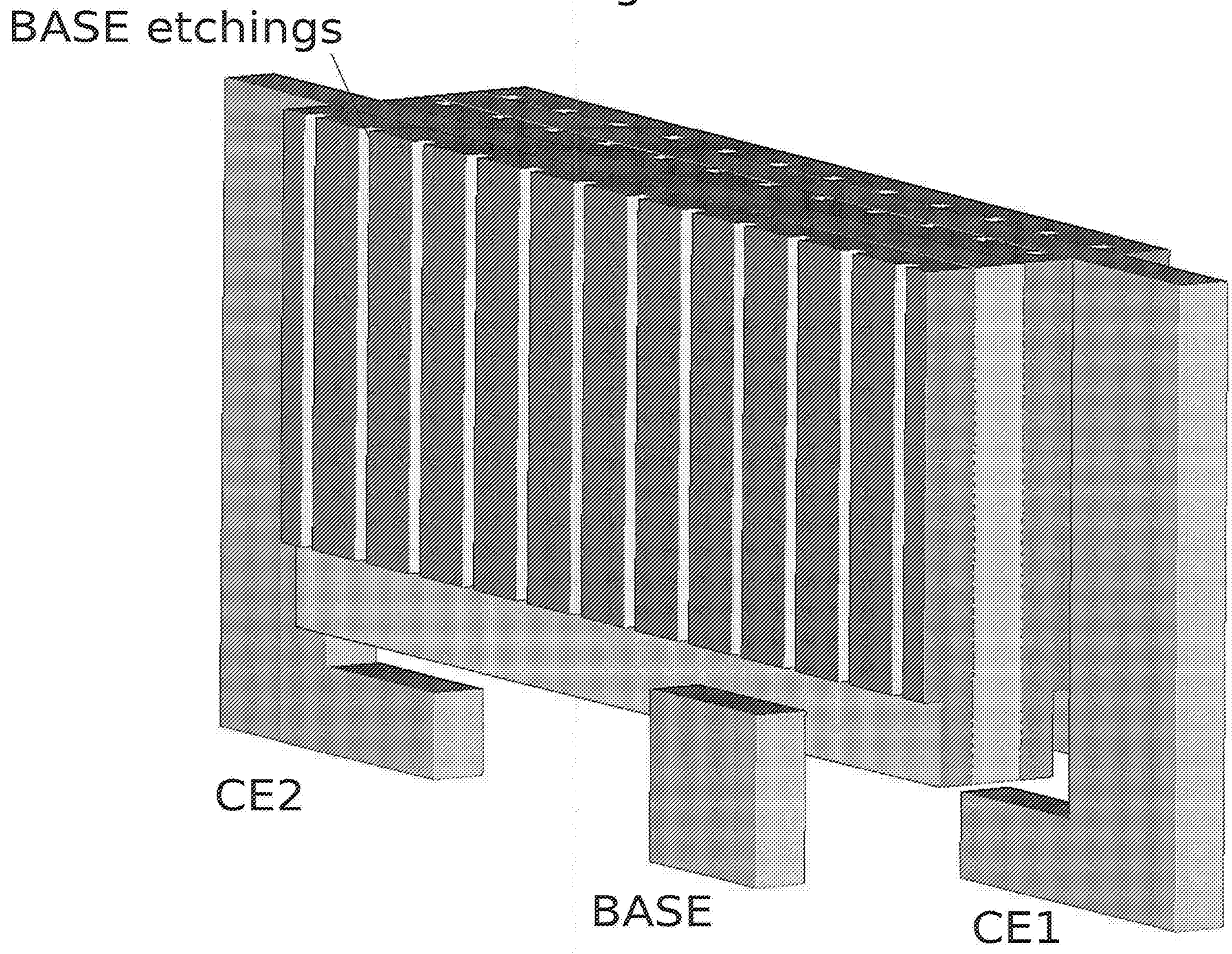
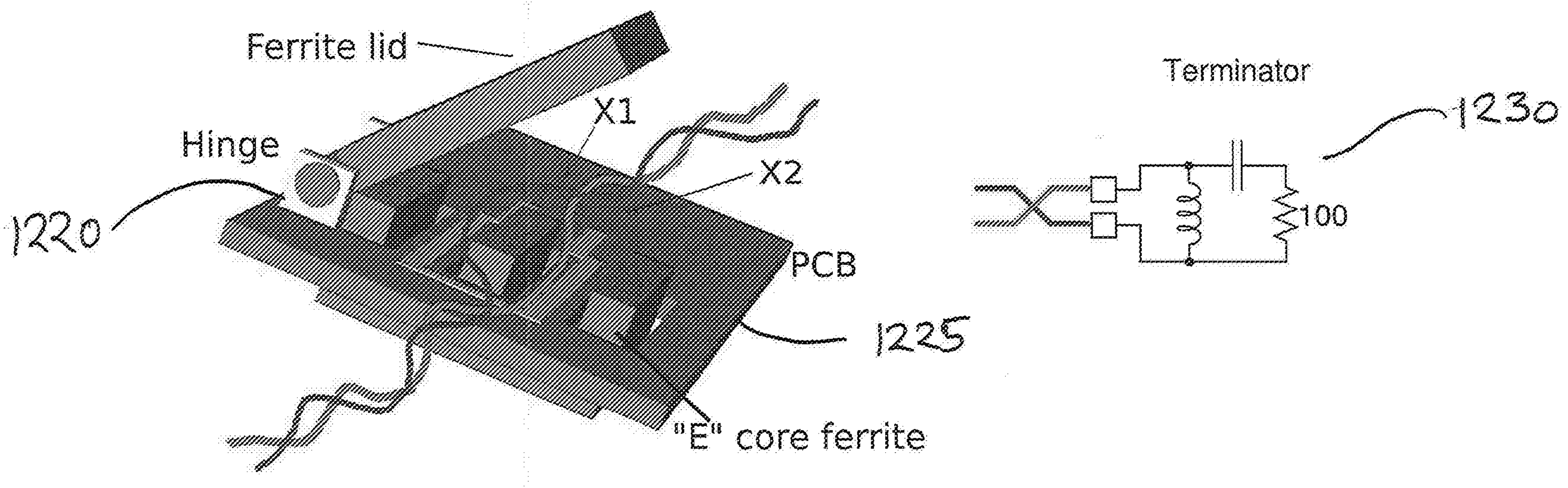


Fig12



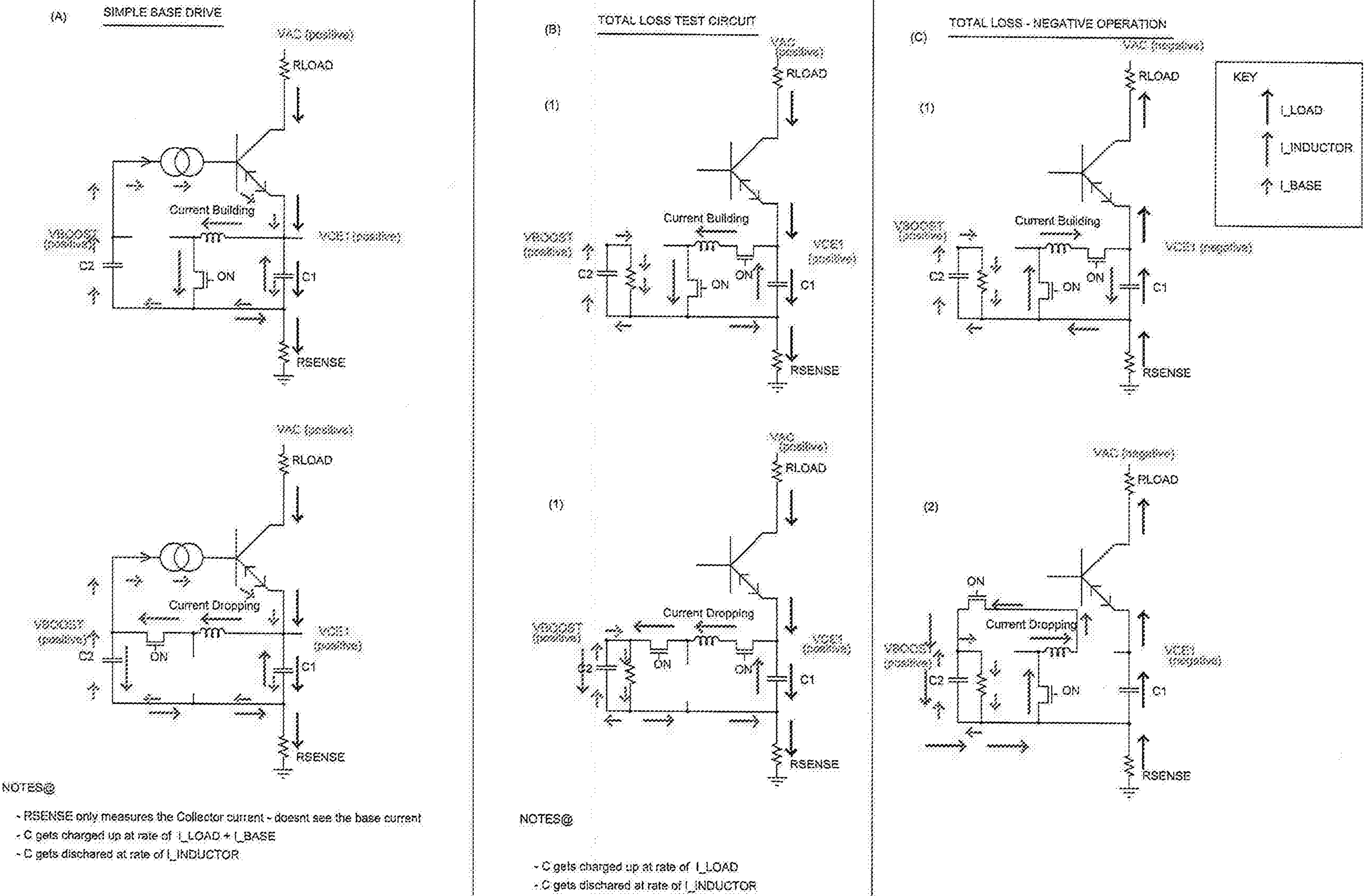
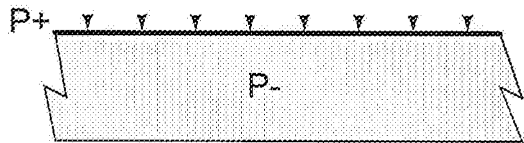


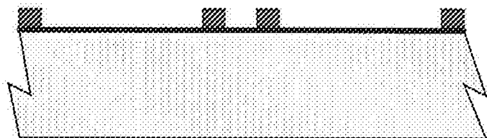
FIG13
(12 of N)
(A)
SIMPLE BASE DRIVE
VAC (positive)
RLOAD
Current Building
VBOOST (positive)
VCE1 (positive)
C2
ON
C1
RSENSE
Current Dropping
NOTES@
- RSENSE only measures the Collector current - doesnt see the base current
- C gets charged up at rate of I_LOAD + I_BASE
- C gets dischared at rate of I_INDUCTOR
(B)
TOTAL LOSS TEST CIRCUIT
(1)
NOTES@
- C gets charged up at rate of I_LOAD
- C gets dischared at rate of I_INDUCTOR
(C)
TOTAL LOSS - NEGATIVE OPERATION
VAC (negative)
VCE1 (negative)
(2)
KEY
I_LOAD
I_INDUCTOR
I_BASE

Fig.14 - PROCESS STEPS for T2-JFET-base Transistor using Nitride

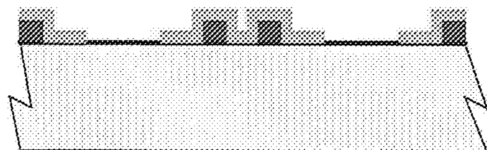
1) Boron Implant (optional)



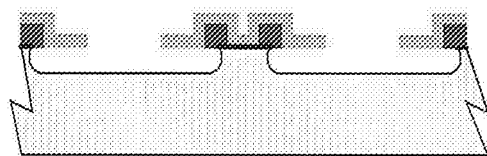
2) SiO2 Pattern



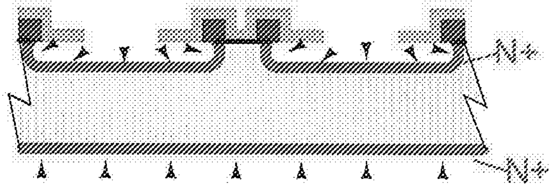
3) Nitride Pattern



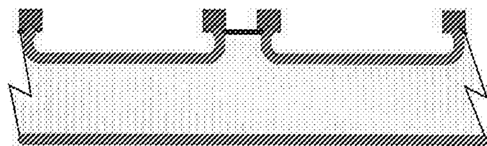
4) Wet (or dry) silicon Etch



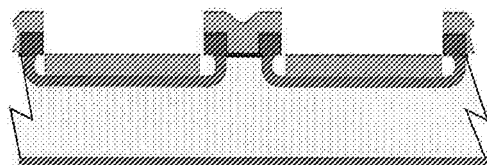
5) Phosphorous Diffusion



6) Nitride Strip



7) Metal Evaporation (self masking)



8) Finished device

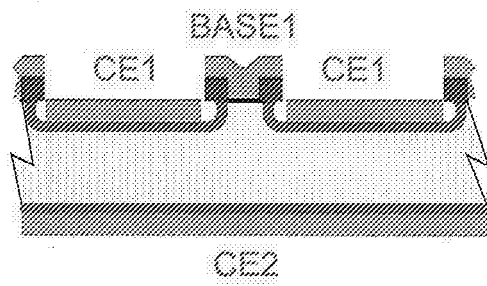


Fig.15 - PROCESS STEPS for T2-JFET-base using Oxide only

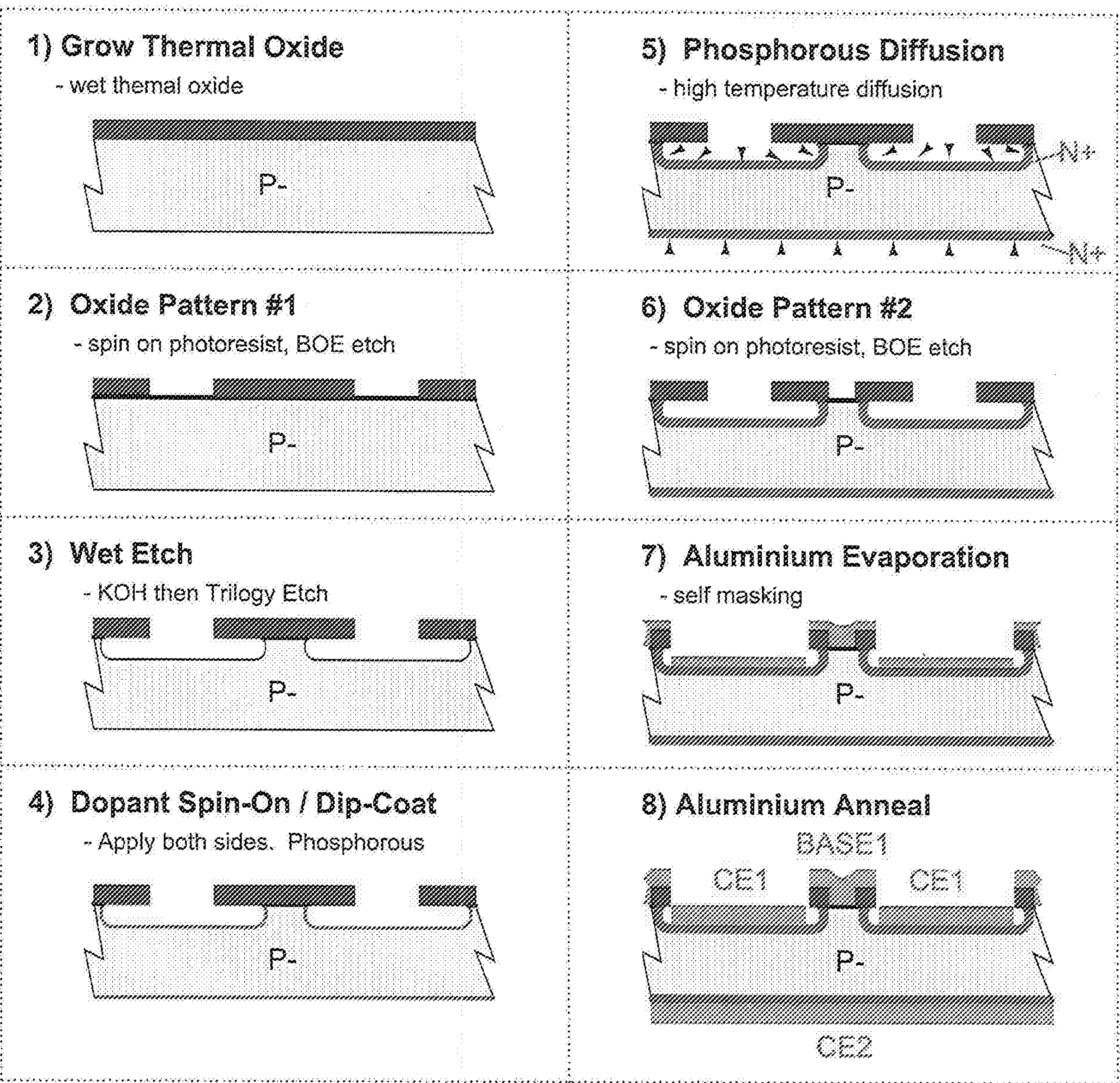


Fig. 16 - PROCESS STEPS for T2 - BJT base using oxide only

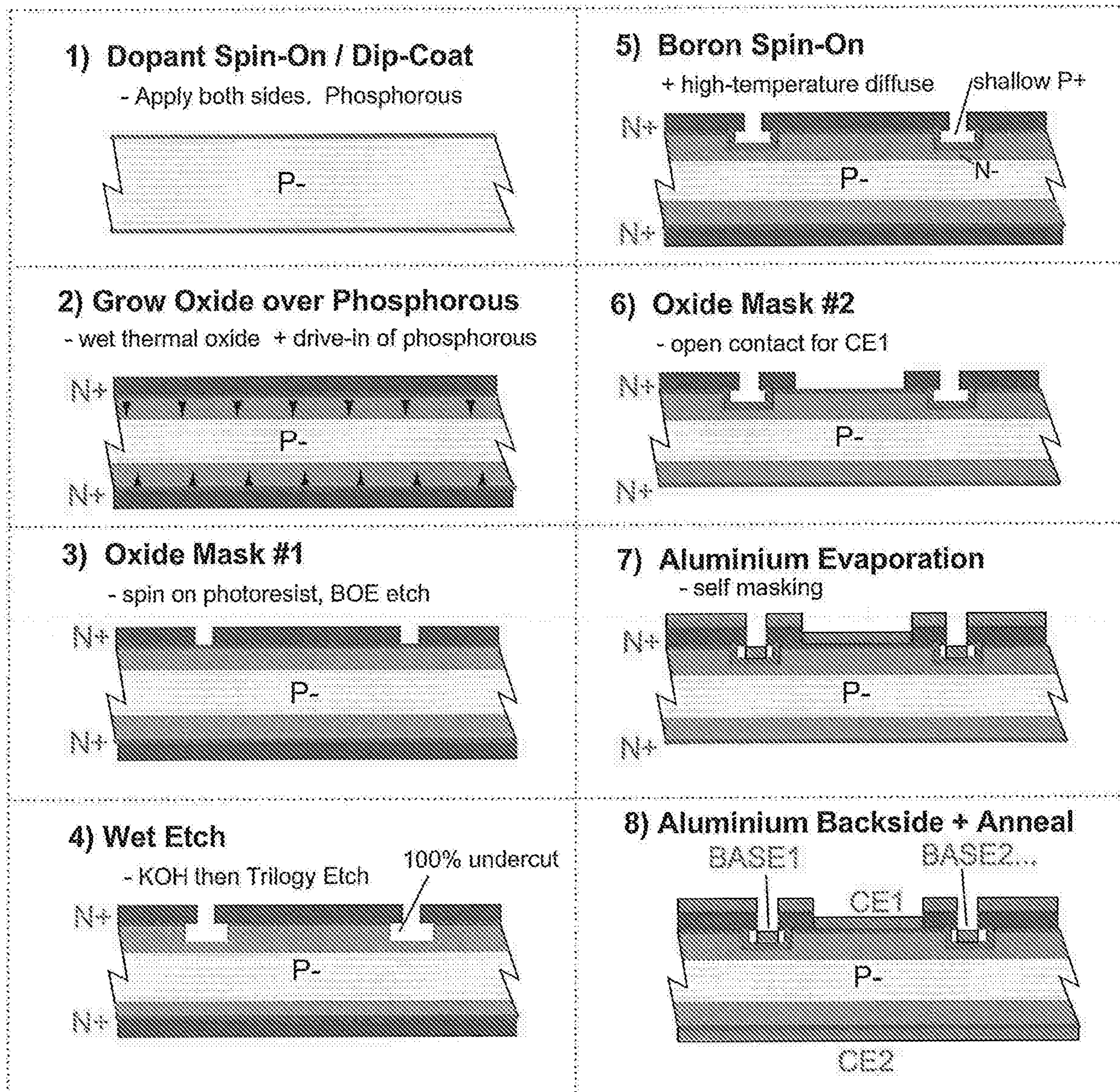


Fig. 17 - SINGLE MASK, T2-BJT base, <100> and <110> etching method

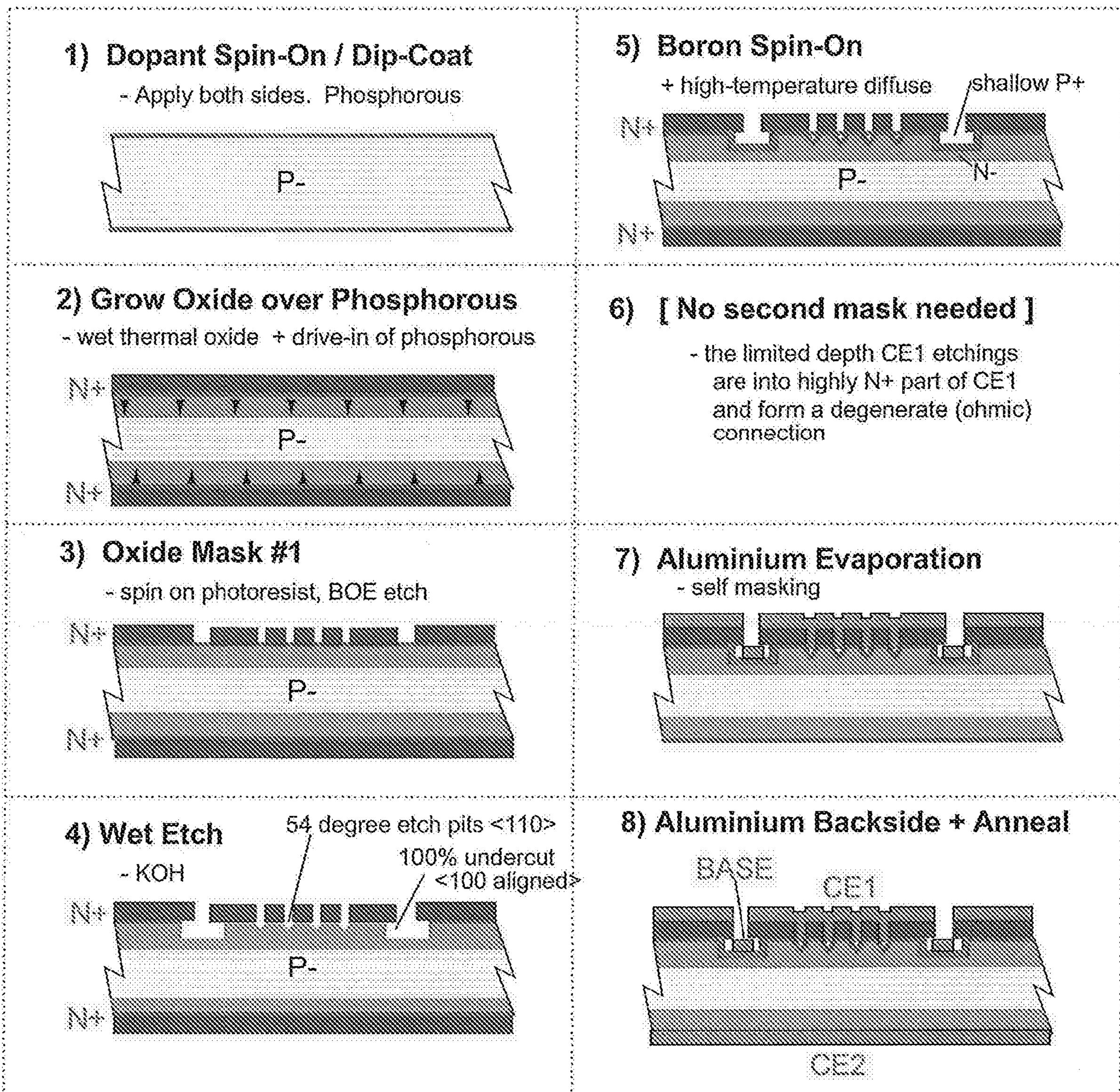


Fig. 18

Single Mask Scheme - with self-limiting contact depth but unrestricted trench depth
using crytalographic anisotropic etch (KOH, TMAH, EDP or similar)

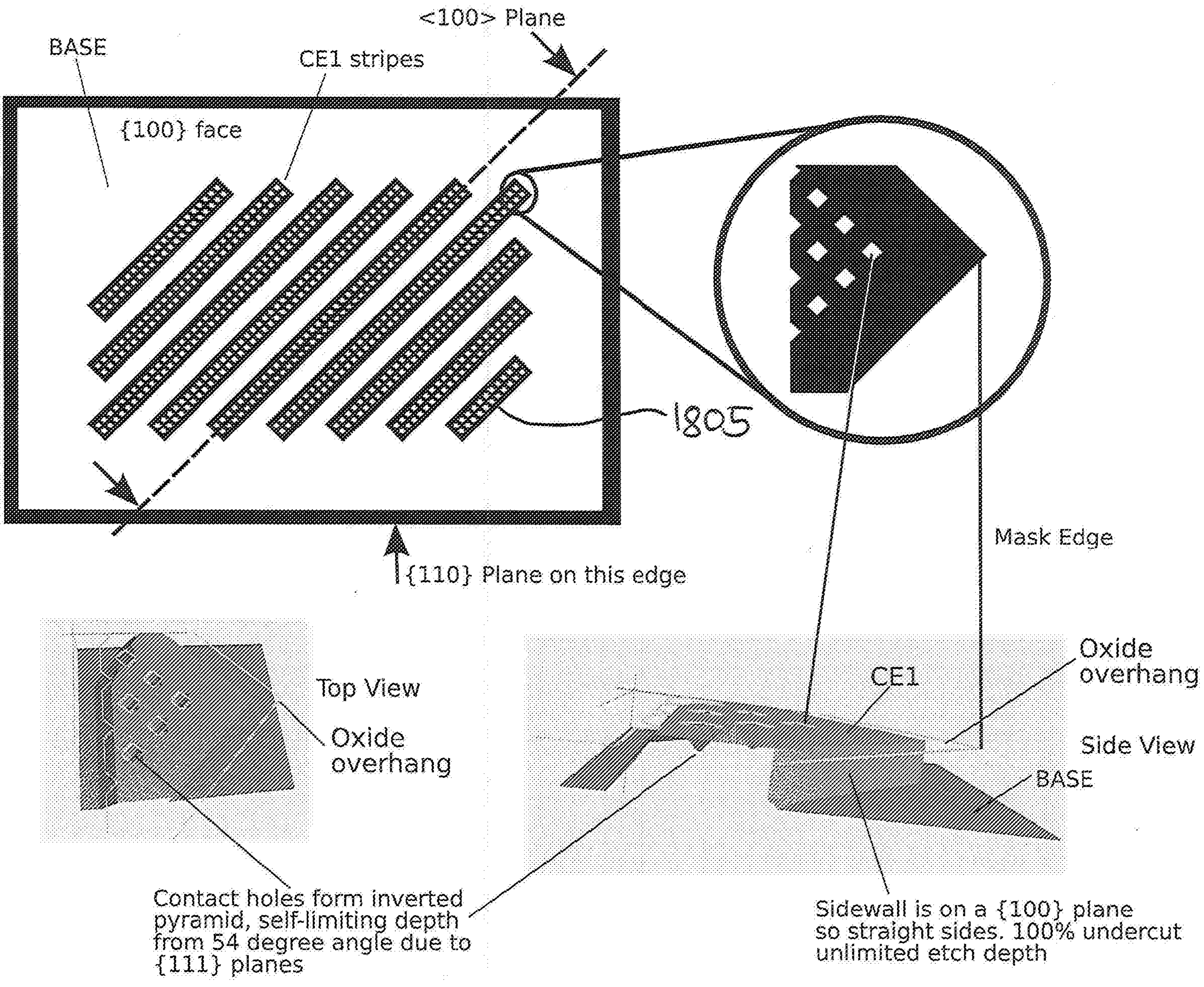
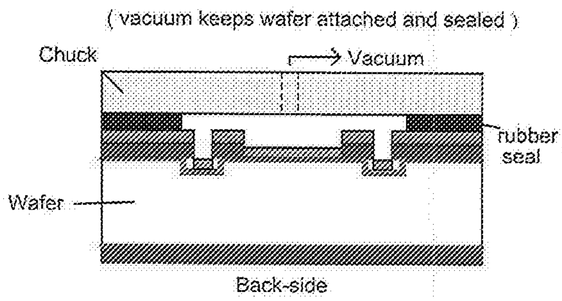


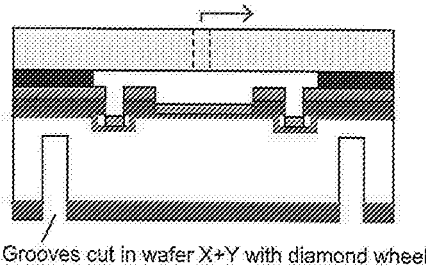
Fig.19 - SINGULATION / BEVEL / PASSIVATION STEPS for THYRISTOR 2.0

9) Mount wafer on holder

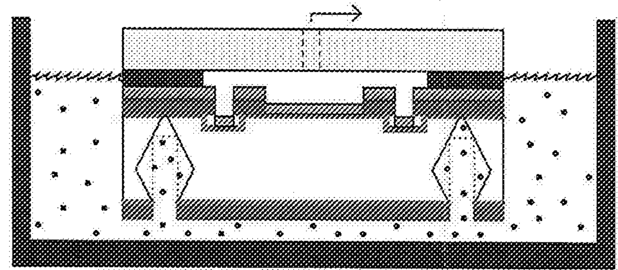
(vacuum keeps wafer attached and sealed)



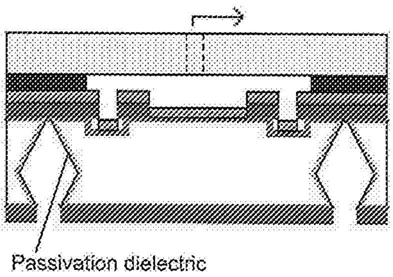
10) Grind singulation slots (X and Y)



11) Anisotropic Wet Etch (e.g. KOH solution)



11) Passivation (CVD or ALD) Al203



Simulation of above using wet-etch atomistic simulator

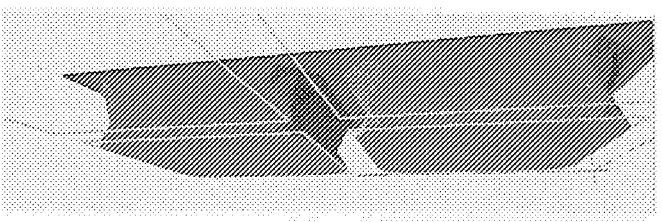
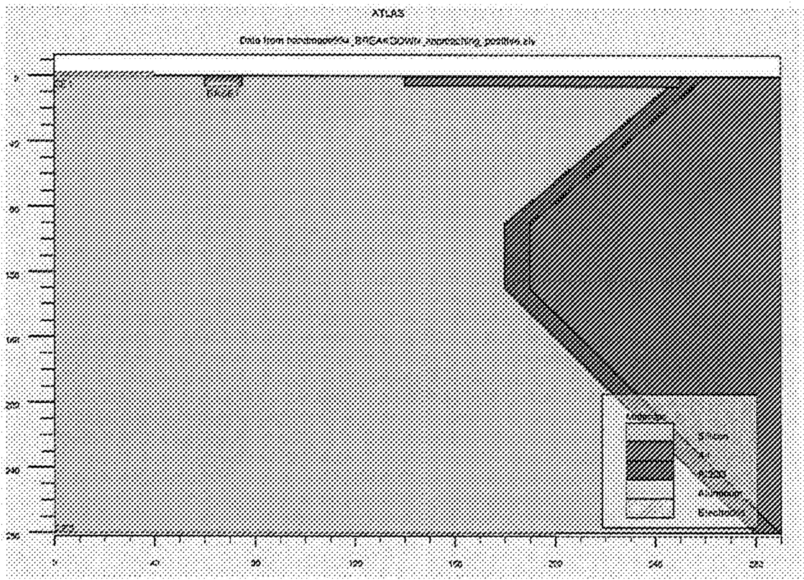
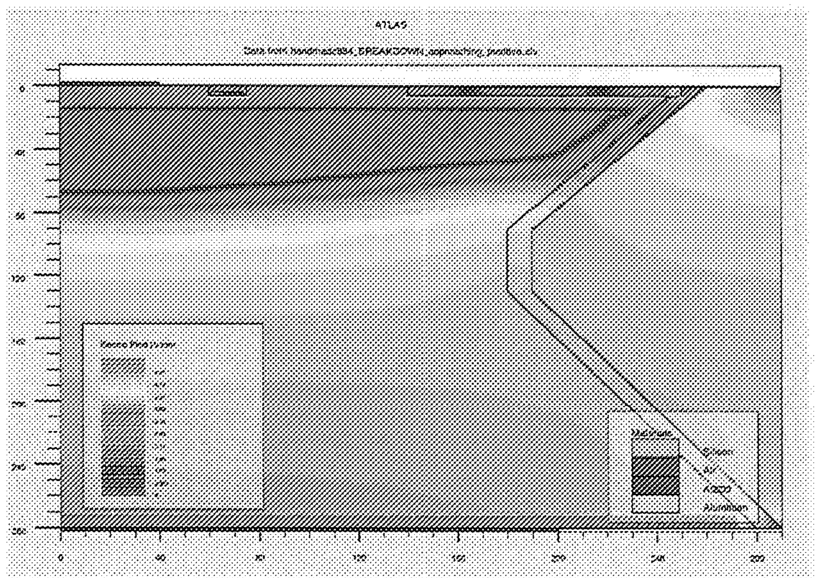


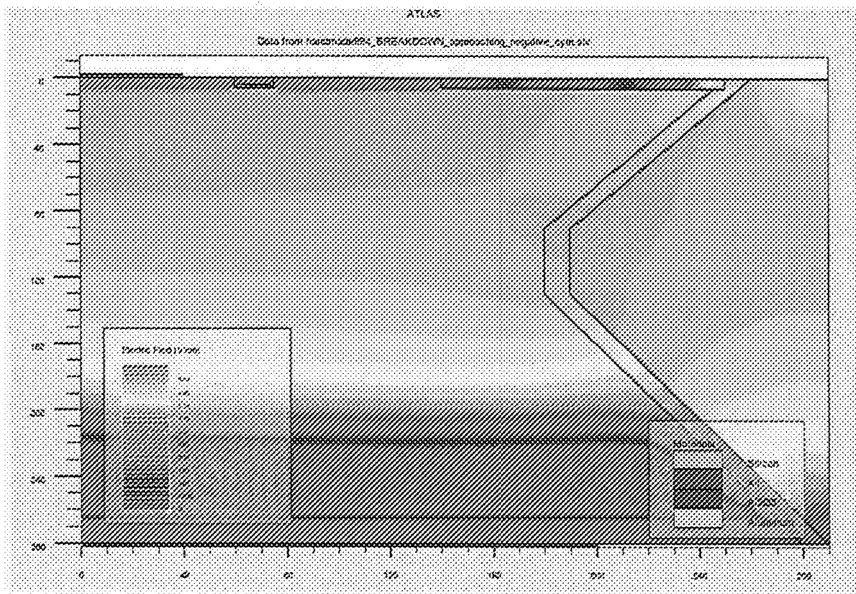
Fig.20



Double Positive Edge layout



CE2 = +1400V electric field map



CE2 = -1400V electric field map

Fig. 21

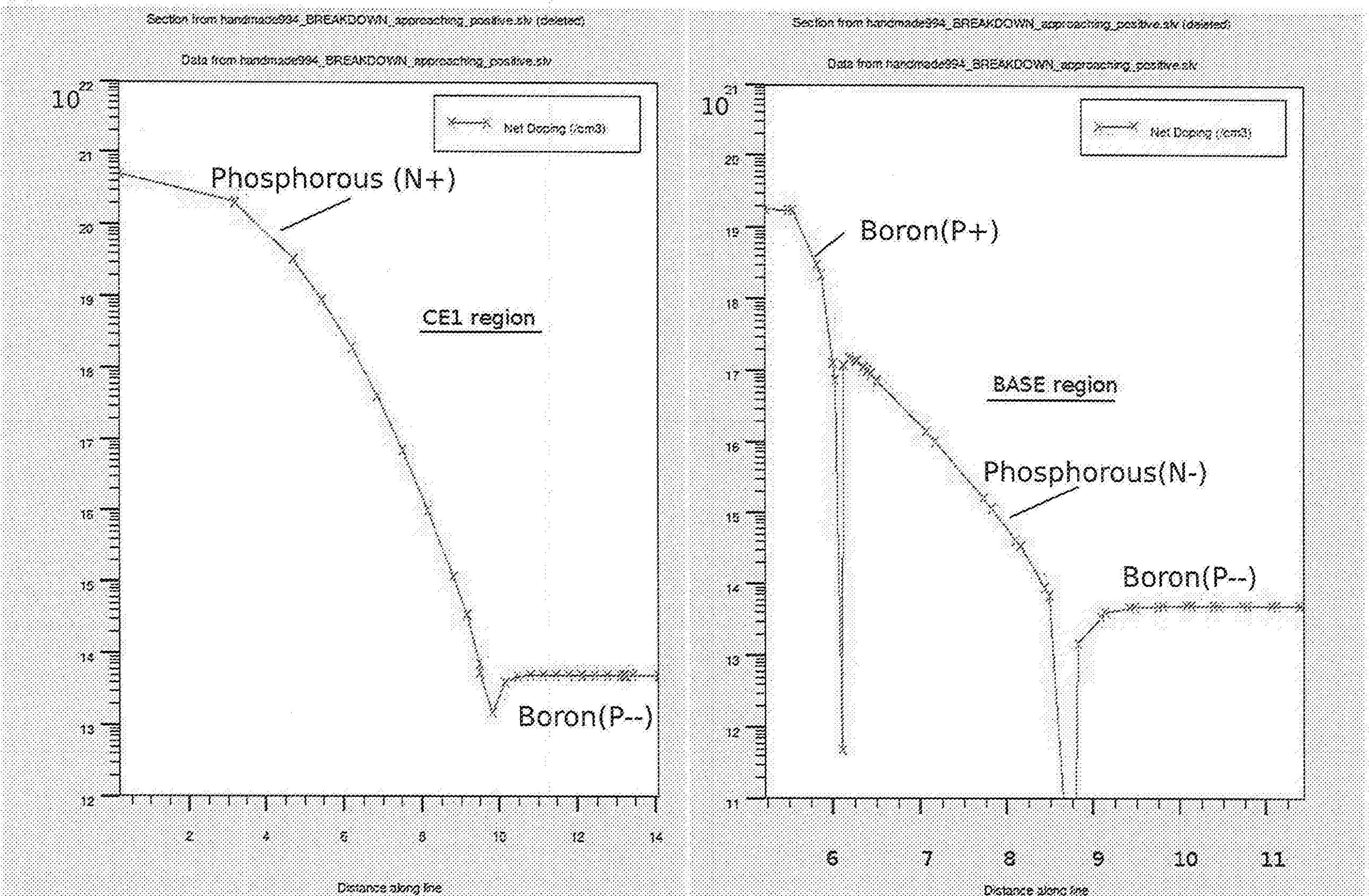
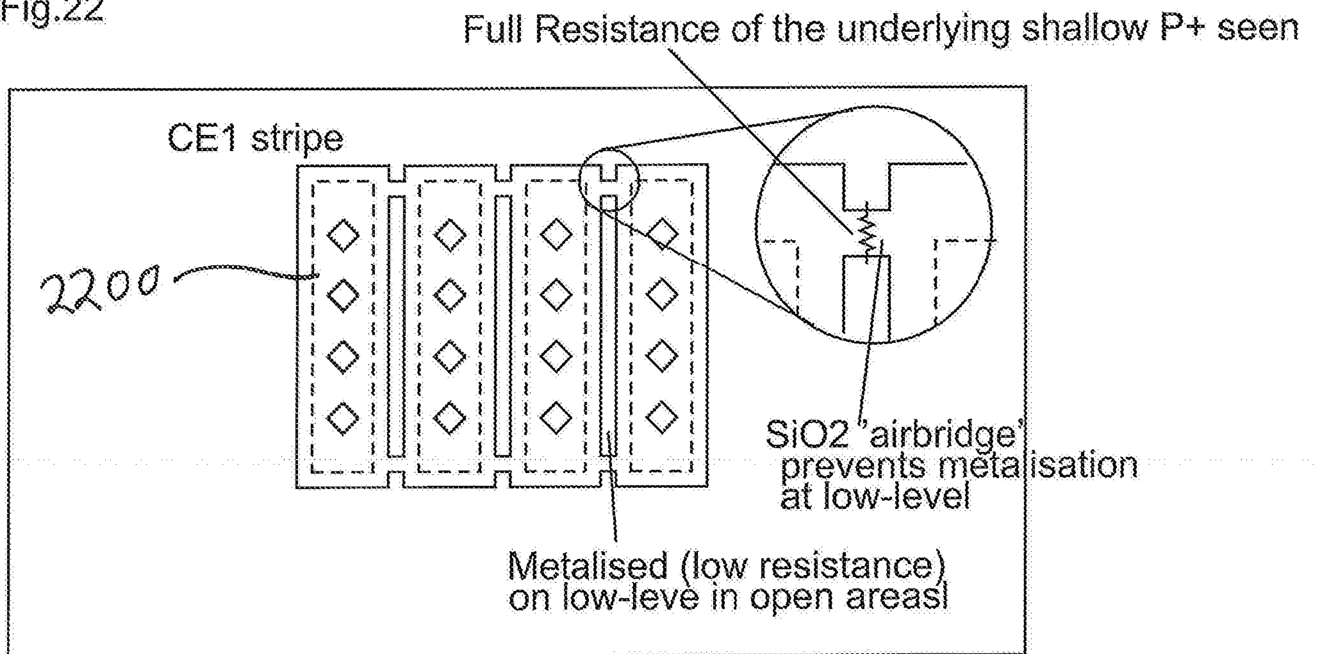


Fig.22



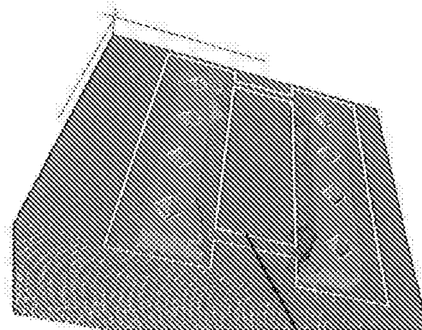


Fig.23

Solid-state relay module including a 'slab' type inductor for bootstrap DCDC

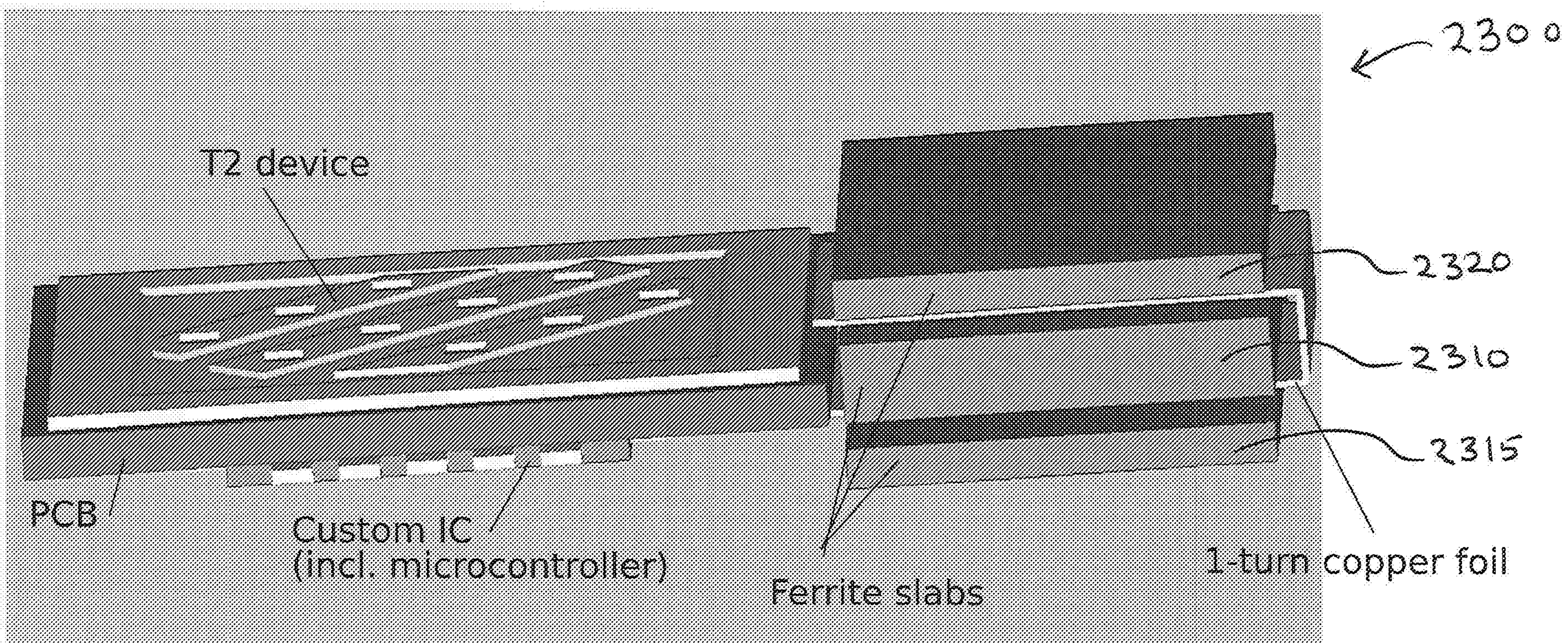


Fig24 A) BJT BASE: DEVICE IS OFF

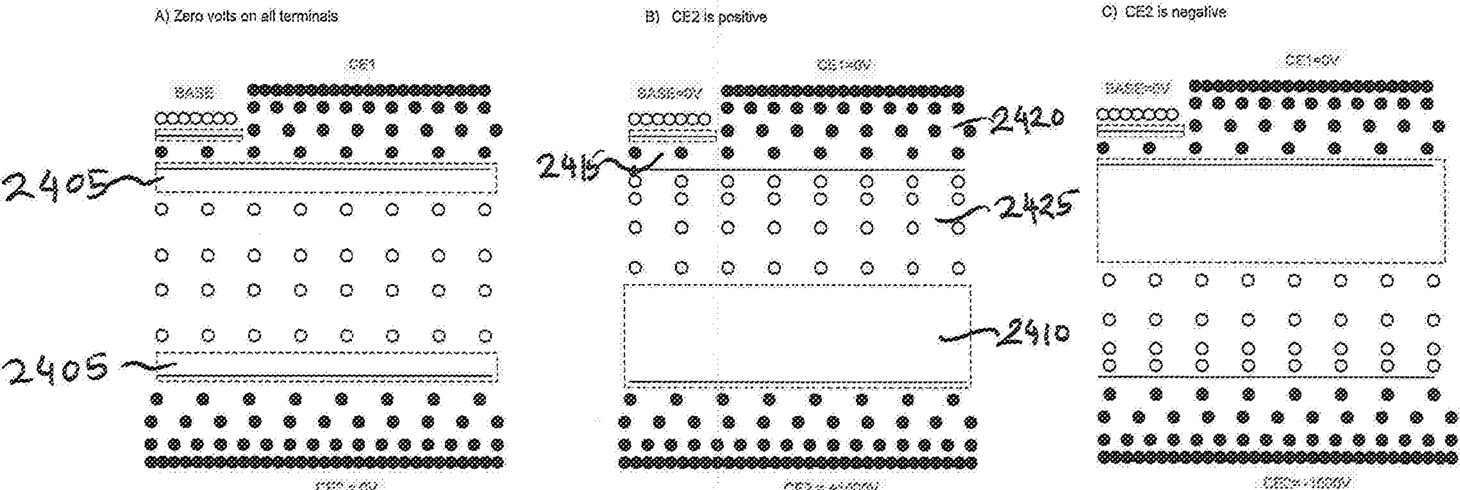


Fig24 B) BJT BASE : DEVICE IS ON

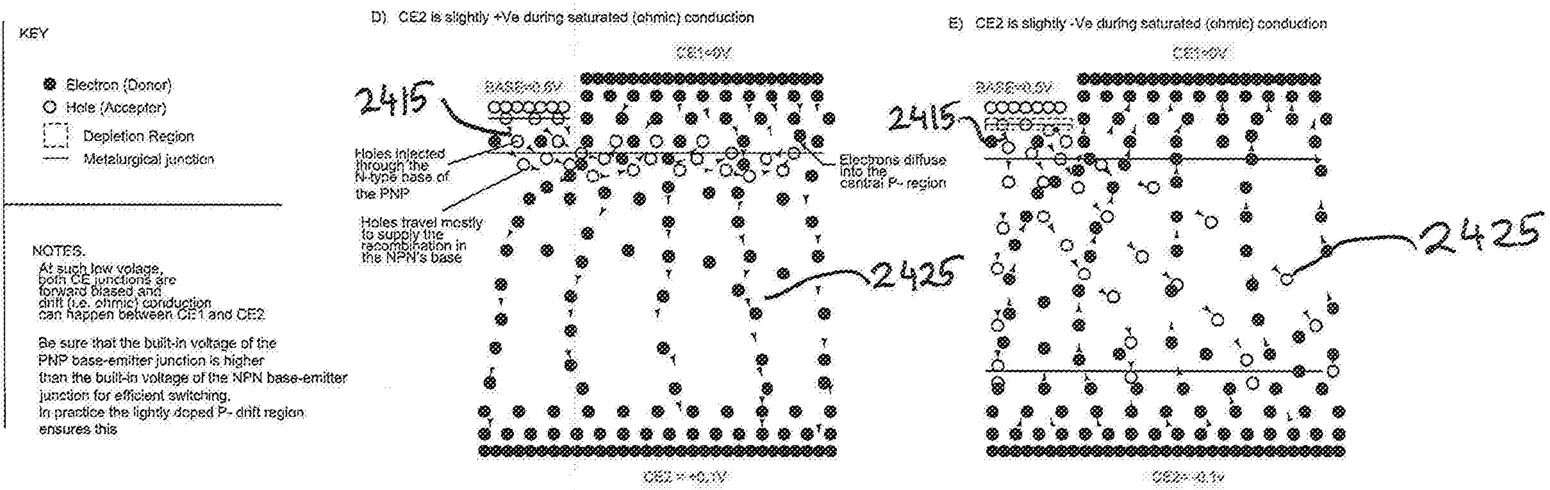


Fig25 A) JFET BASE - DEVICE IS OFF

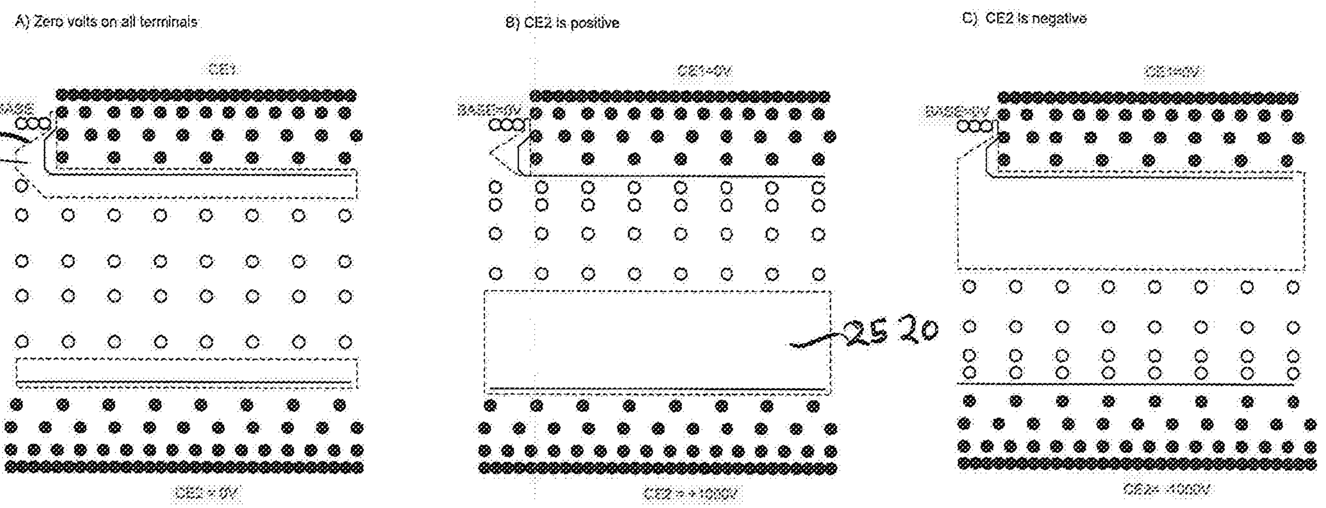


Fig25 B) JFET-BASE - DEVICE IS ON

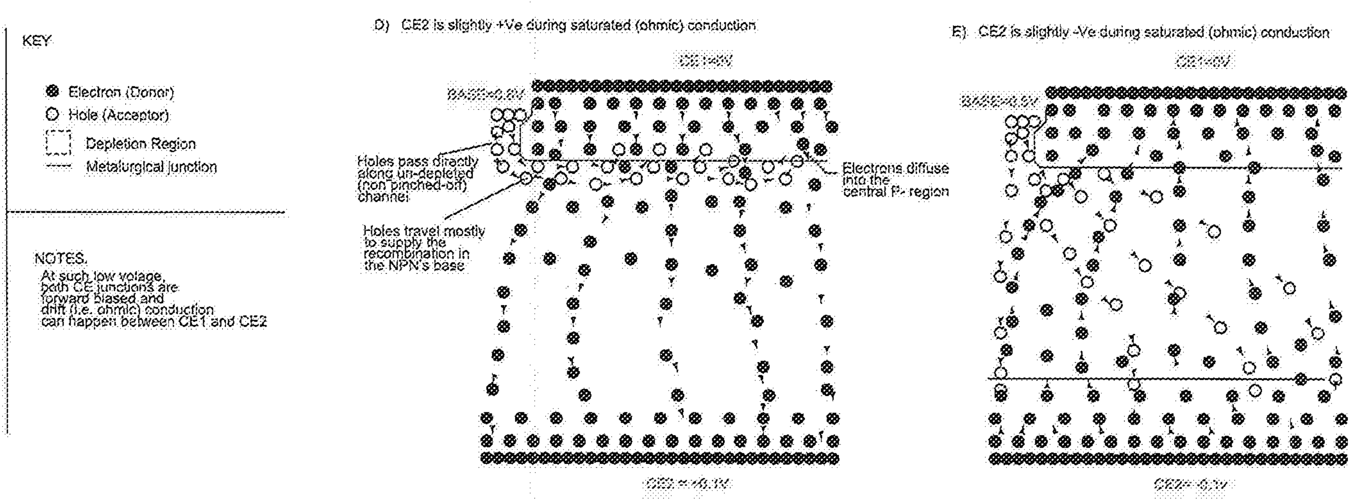
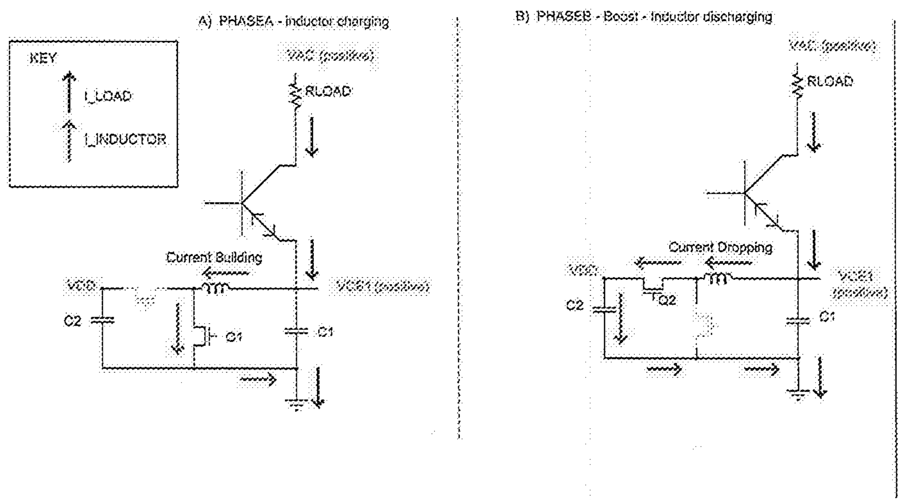
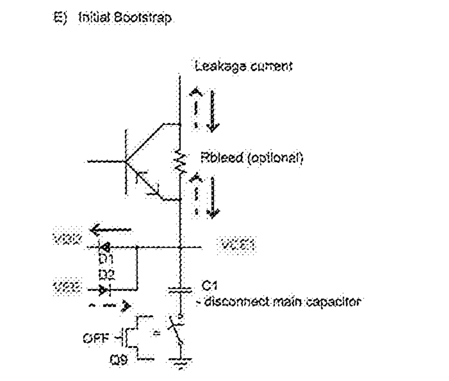
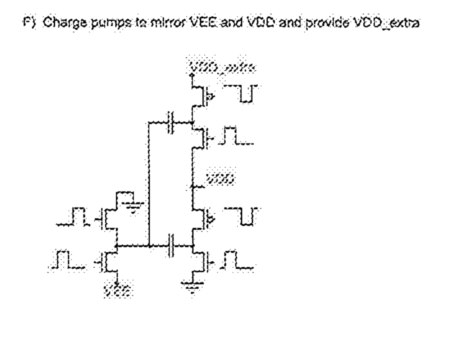


Fig26 Bootstrap, Chargepumps and Base drive circuits

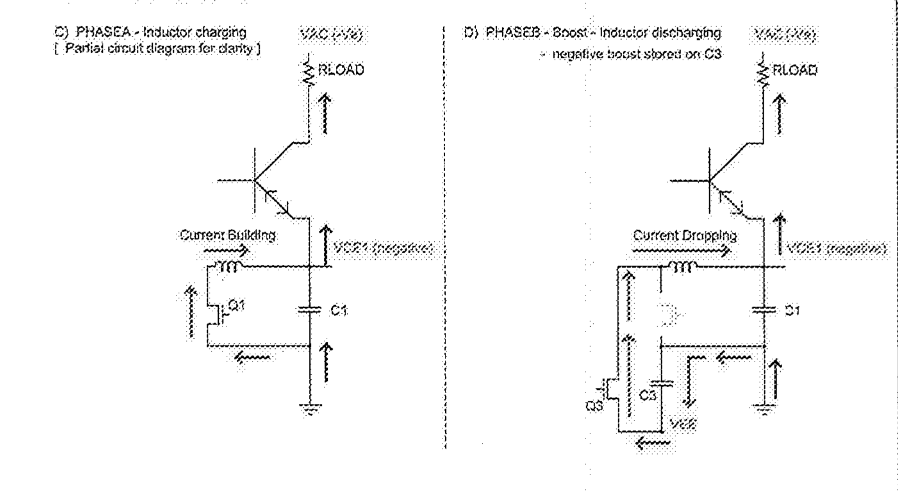
POSITIVE OPERATION







NEGATIVE OPERATION



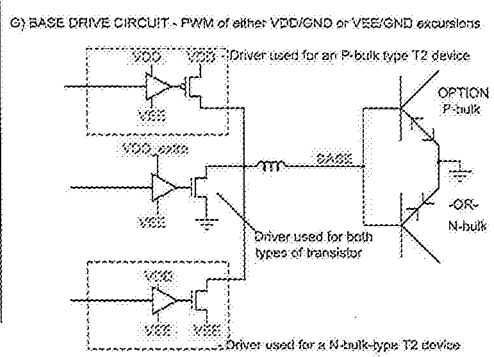
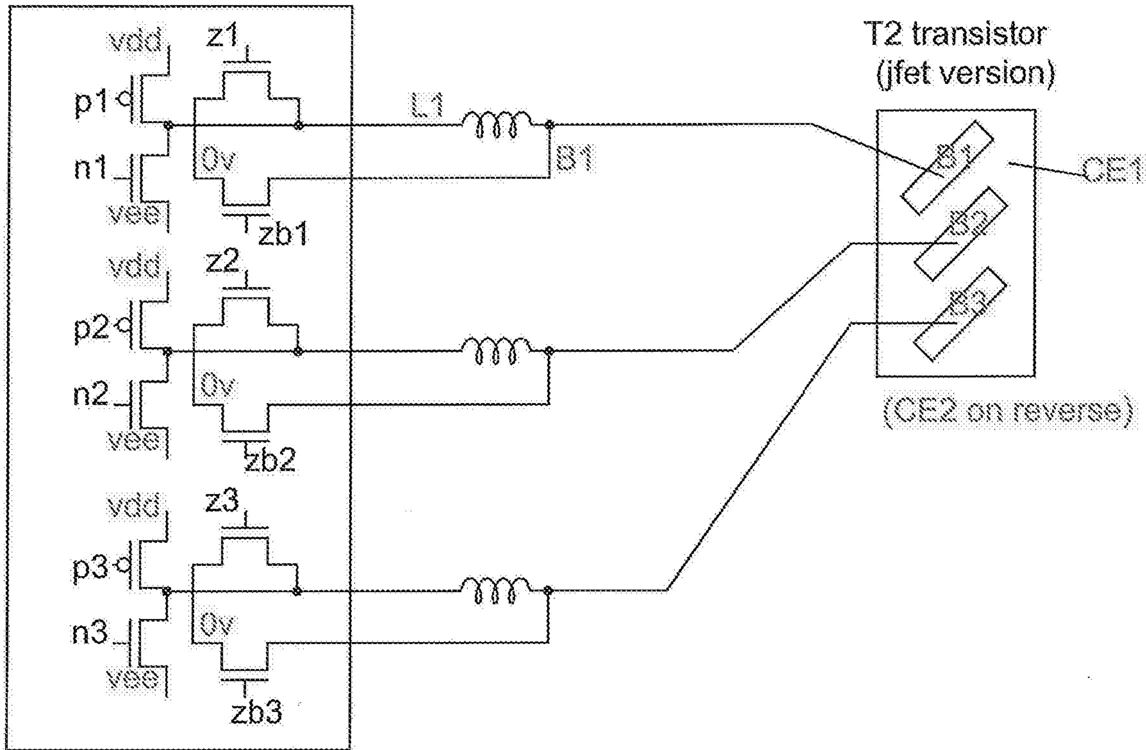
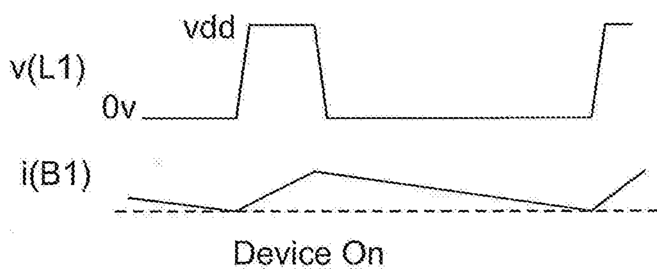


Fig27

A) Multi-output inductive base drive

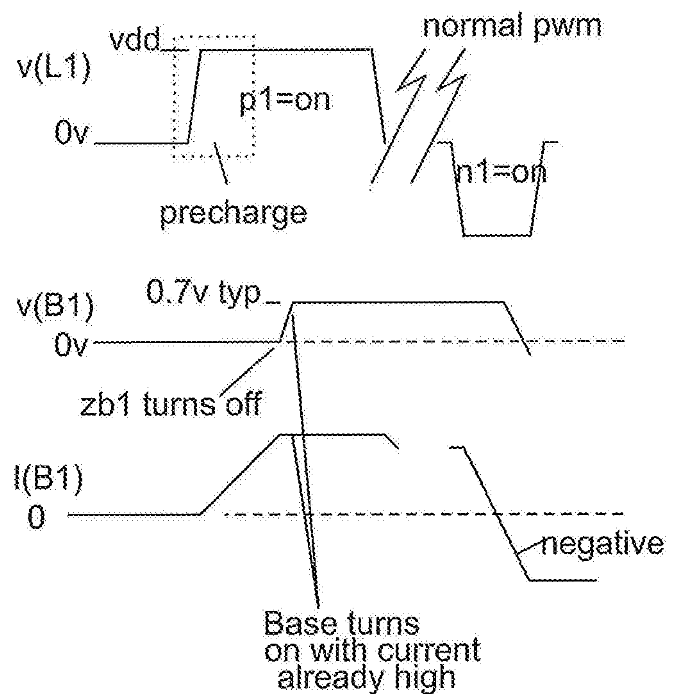


B) example voltage waveforms (repeating)



L2,B2, and L3,B3 are phase-shifted versions of above, moved by 120 degrees

C) base pulse using precharge and discharge



Base 'Finger' driver - one channel

- for PNP based devices (-ve base current)

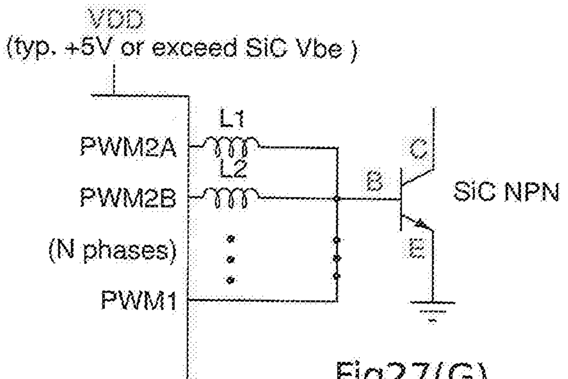


Fig27(D)

- for NPN based devices (+ve base current)

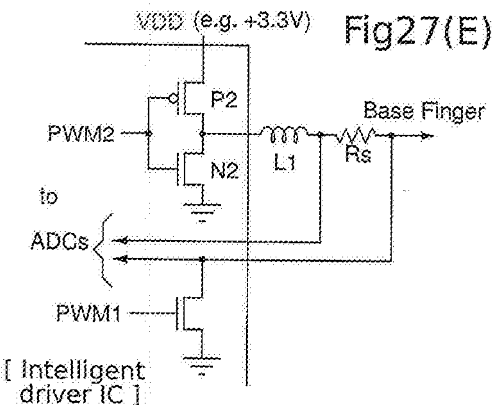


Fig27(E)

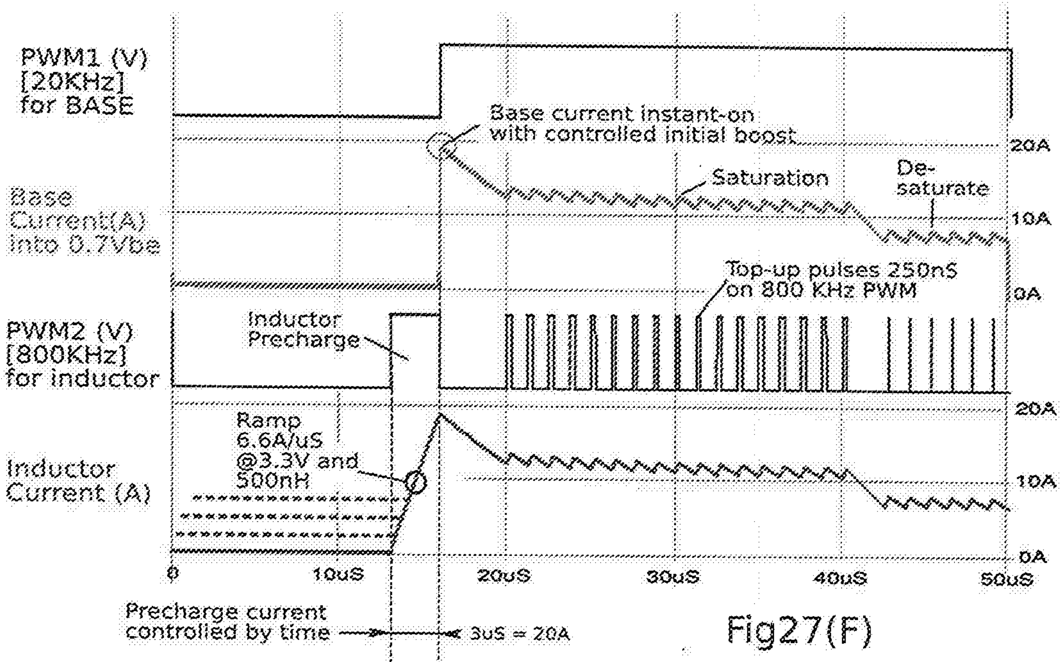


Fig27(F)

Multiphase operation single-base connection

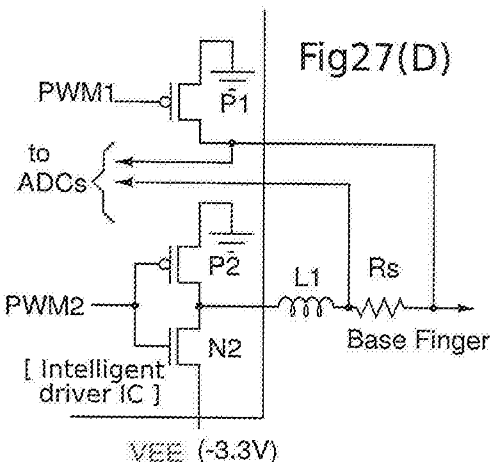


Fig27(G)

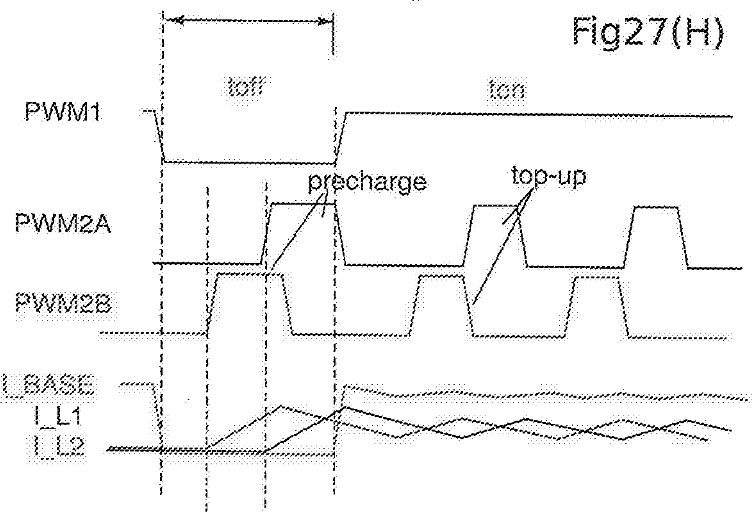


Fig27(H)

Fig28

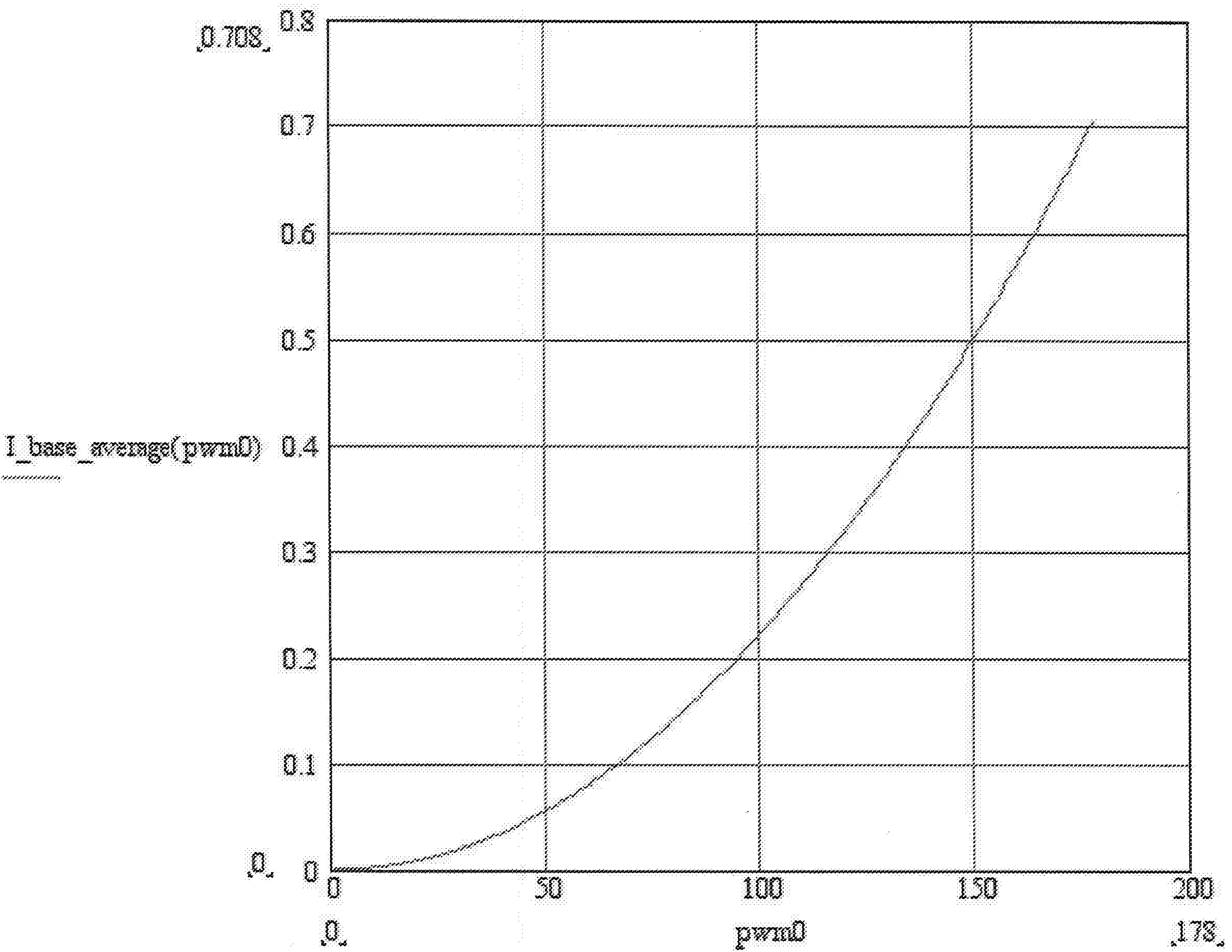


Fig.29 - Programable DAC base drivers - multi-channel

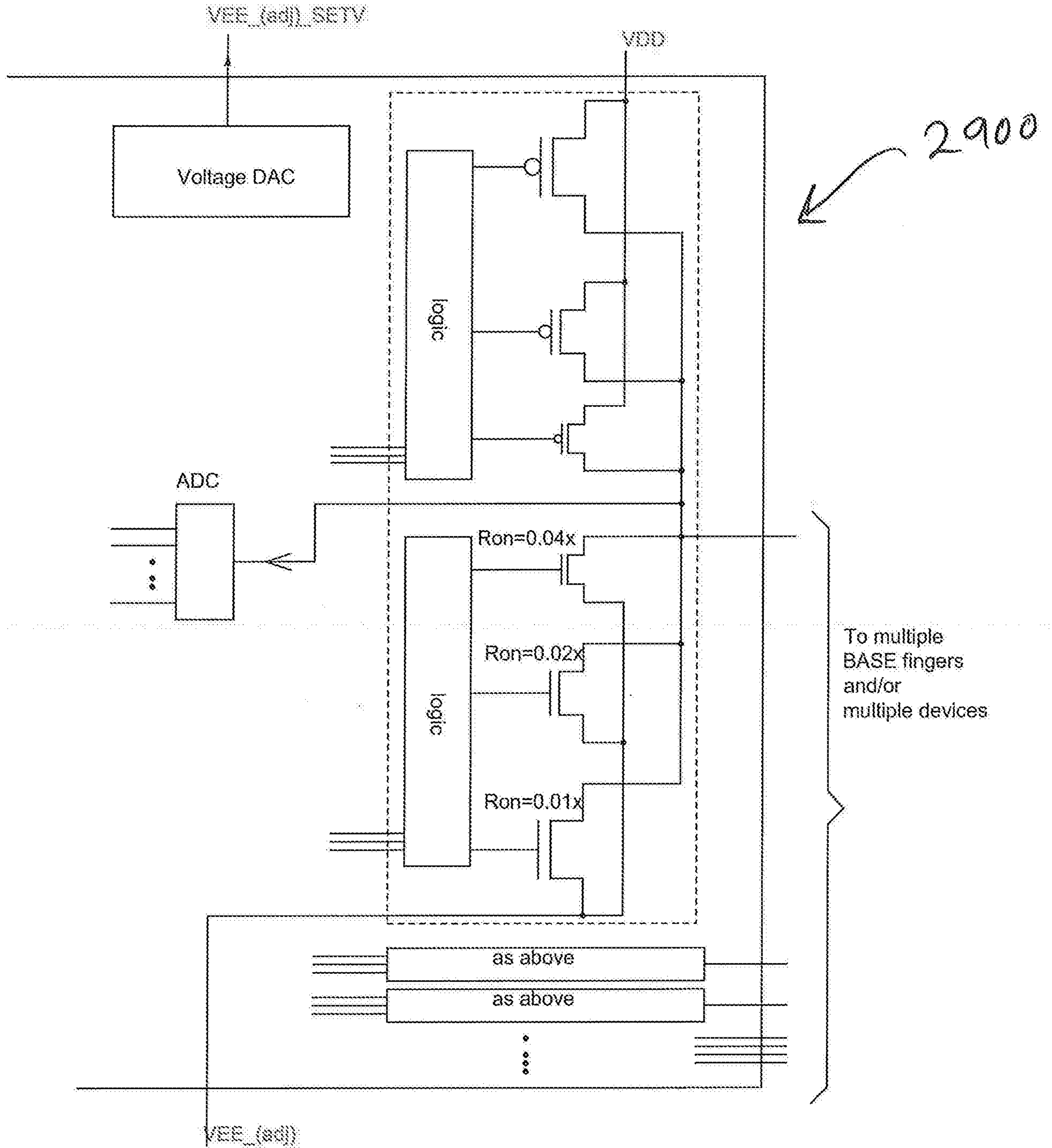
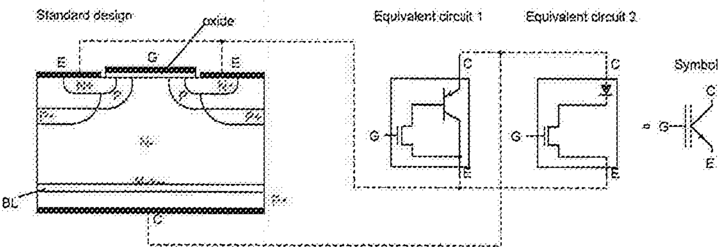
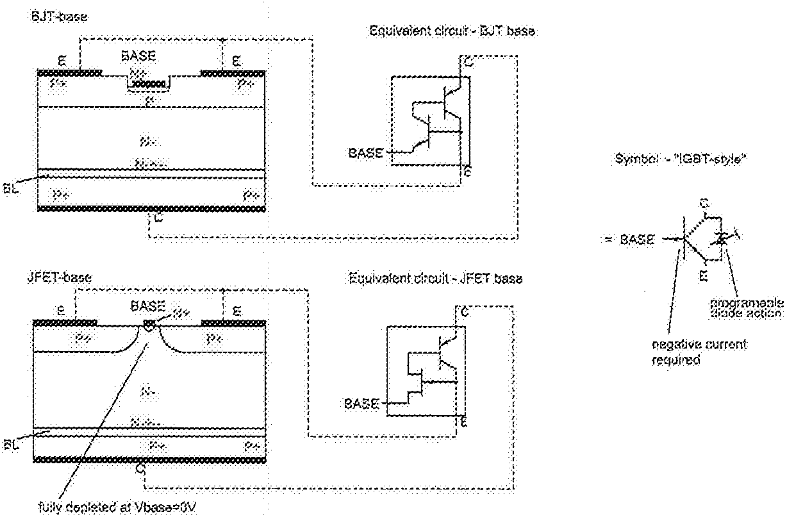


Fig.30

A) IGBT

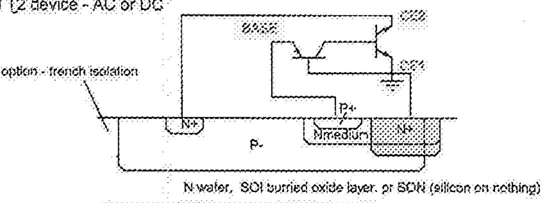


B) I2 device "NIGBT" - AC or DC



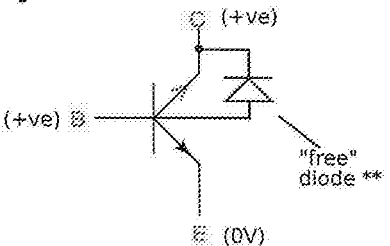
NOTE: BL means burried layer and is optional

(C) Lateral T2 device - AC or DC



B2 device
BJT NPN
Field-Stop

Symbol



** when used with CMOS driver

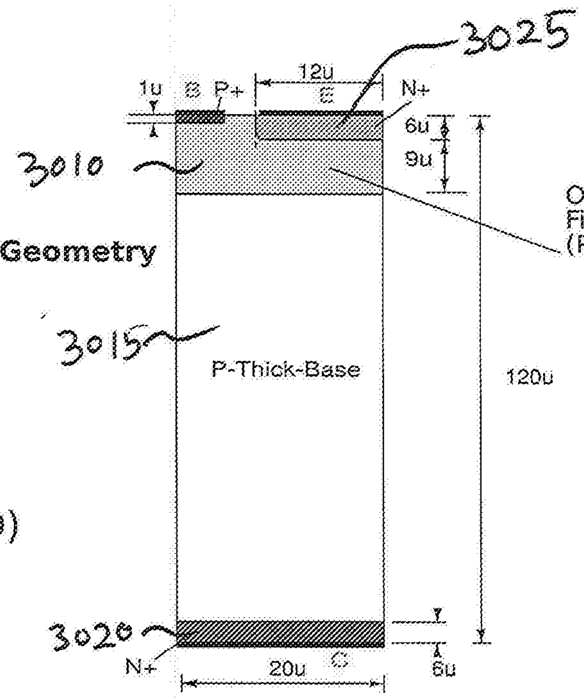


Fig30(D)

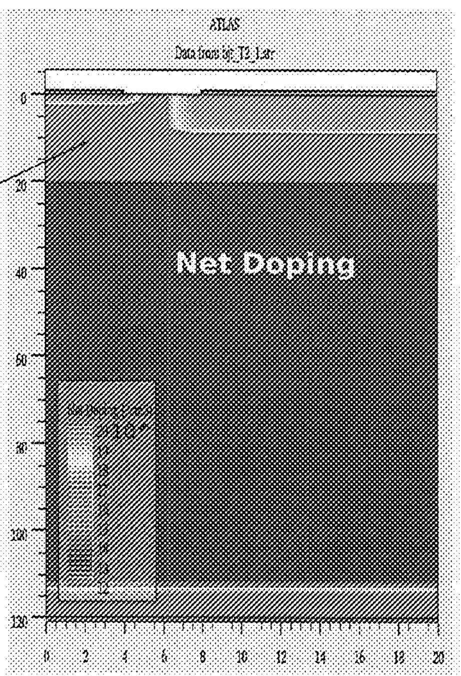


Fig30(E)

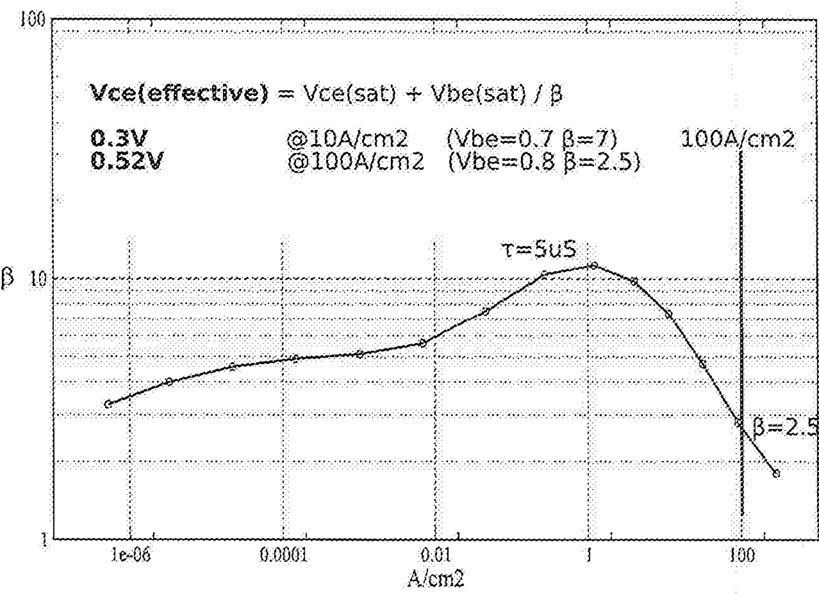


Fig30(F)

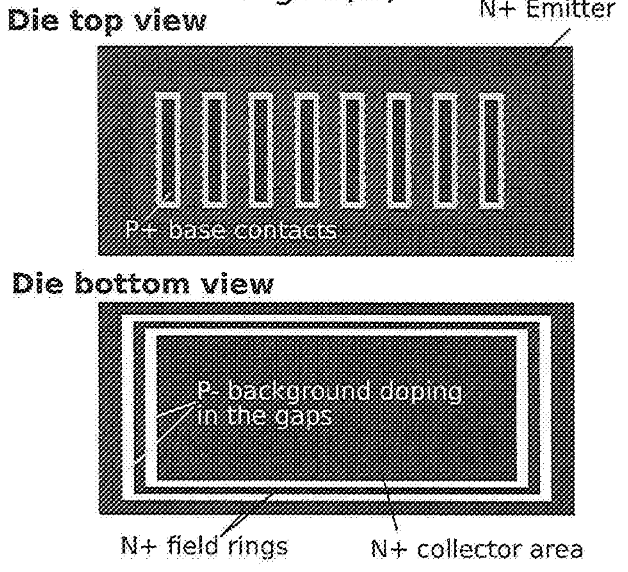
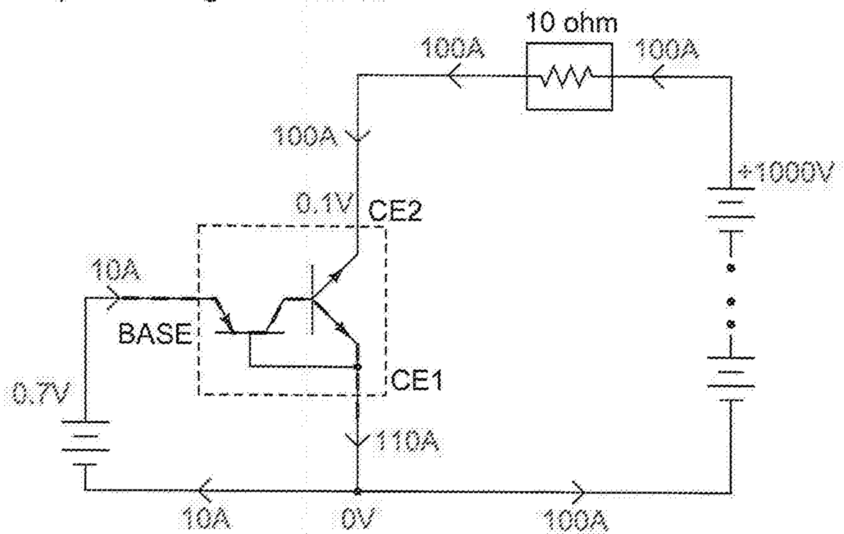


Fig30(G)

Fig.31

A) Conducting a +Ve current



B) Conducting a -Ve current

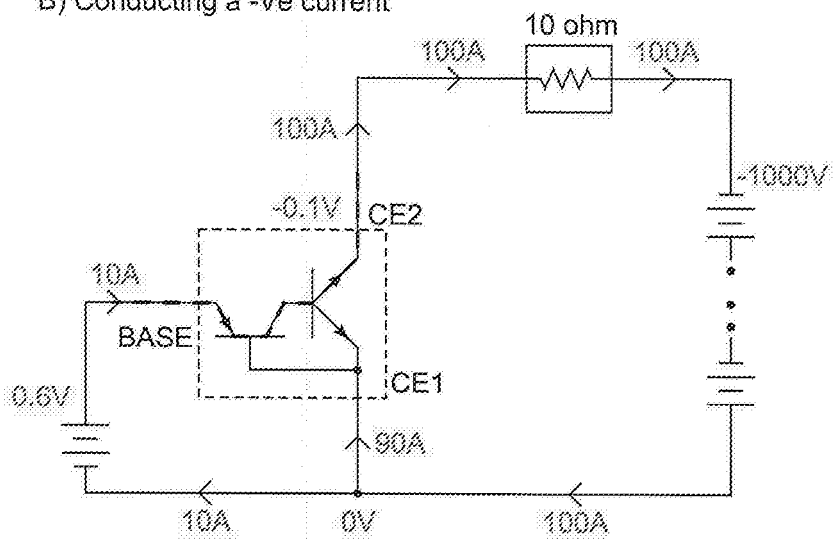
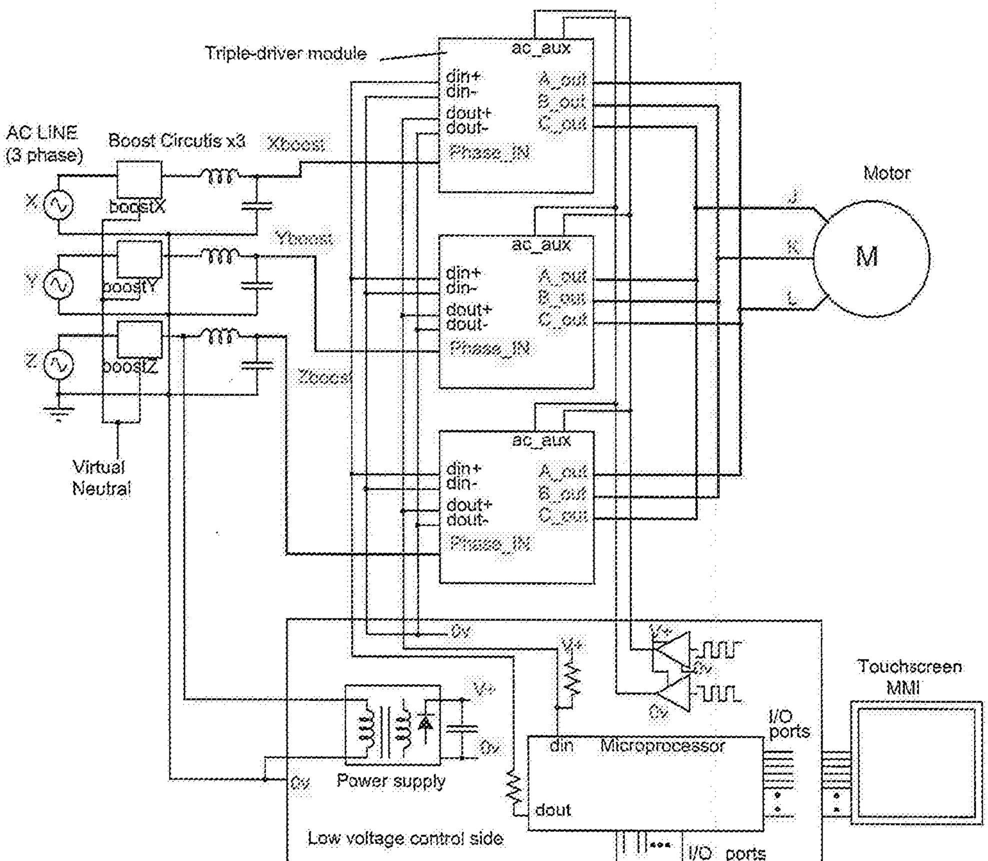
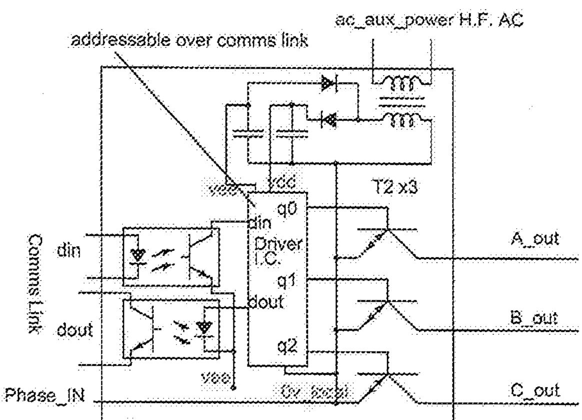


FIG32

A) VARIABLE FREQUENCY MATRIX-CONVERTER DRIVE SYSTEM



B) TRIPLE DRIVER MODULE - Internals



Simplified internals diagram of triple-T2 driver module
- not shown are A-D, D-A I/O, Microcontroller features which were previously shown on single-channel drivers and can obviously be applied here to all 3 switches

C) BOOST CIRCUIT (AC/AC transformer - concept drawing)

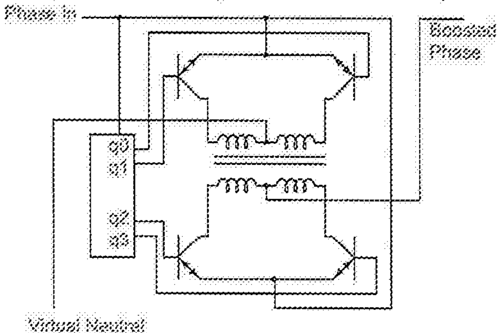


FIG 33(A)

3D stack for Driver IC, Discretes and Power transistor for integrated-driver module

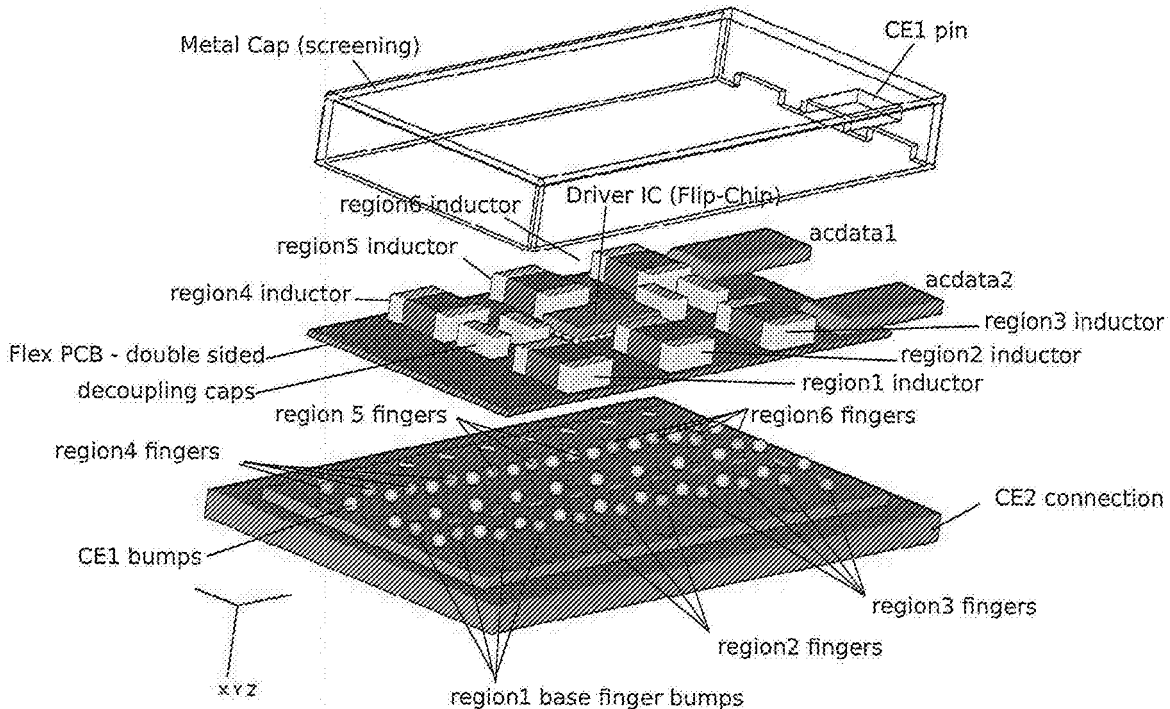


FIG 33(B)

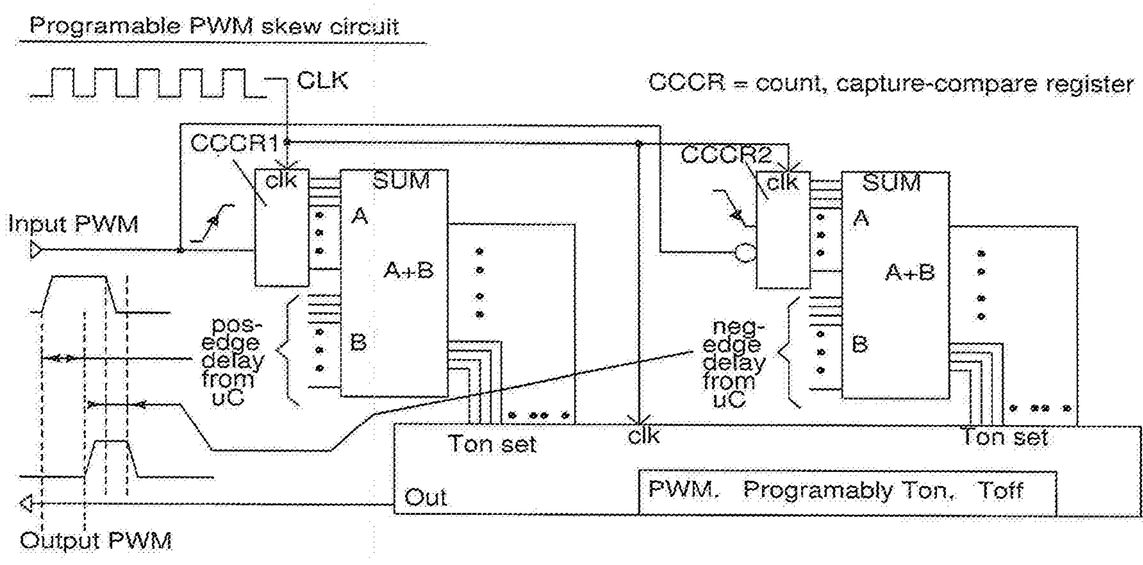


Fig 34 - low leakage relay switches

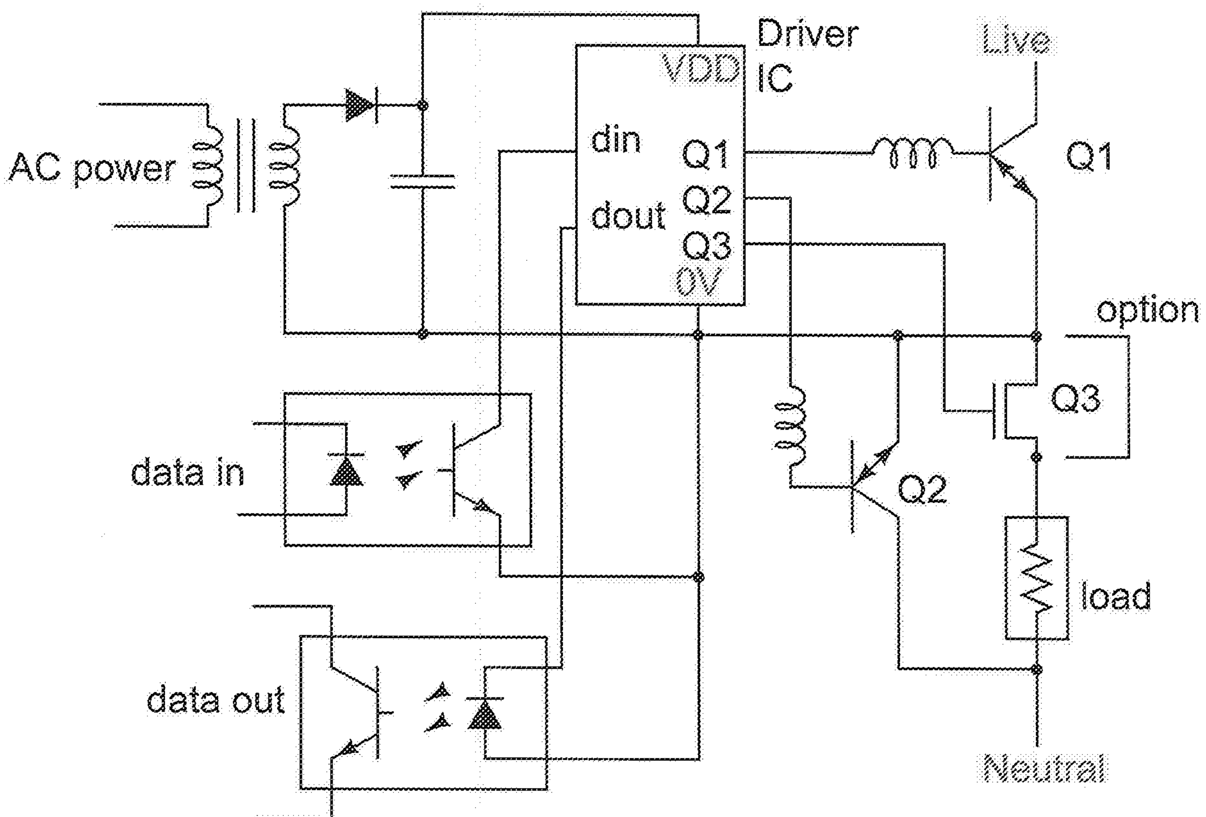


Fig35A NMOS vertical conduction on modified CMOS

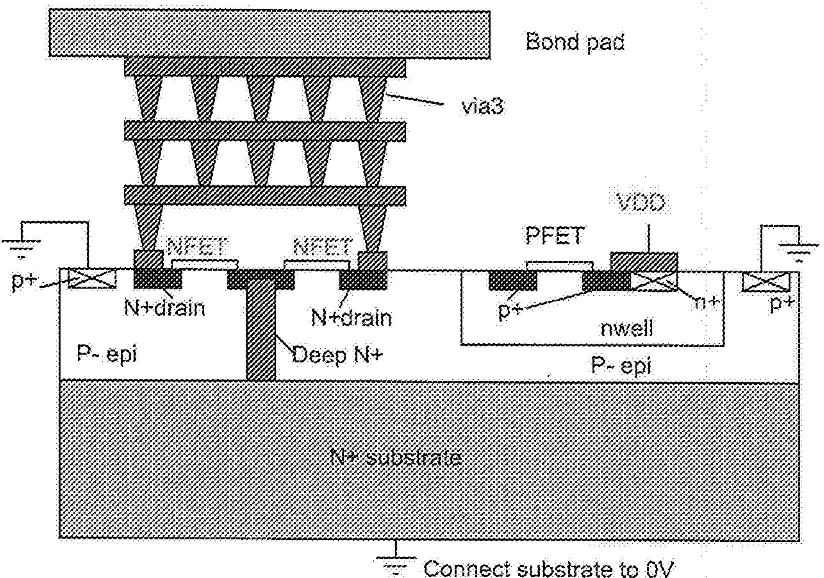


Fig35B Syncronous rectifier from transformer with 2-way dataflow

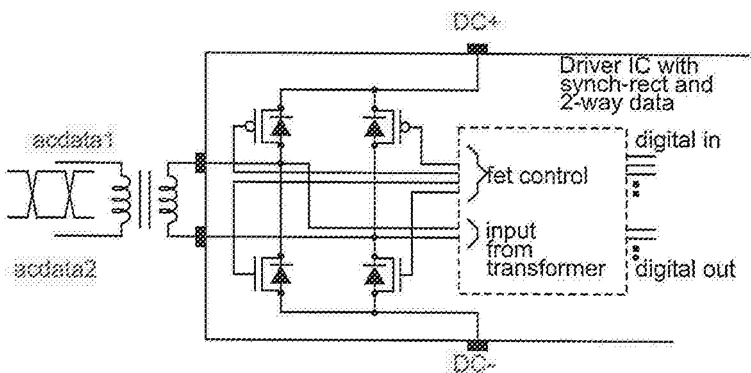
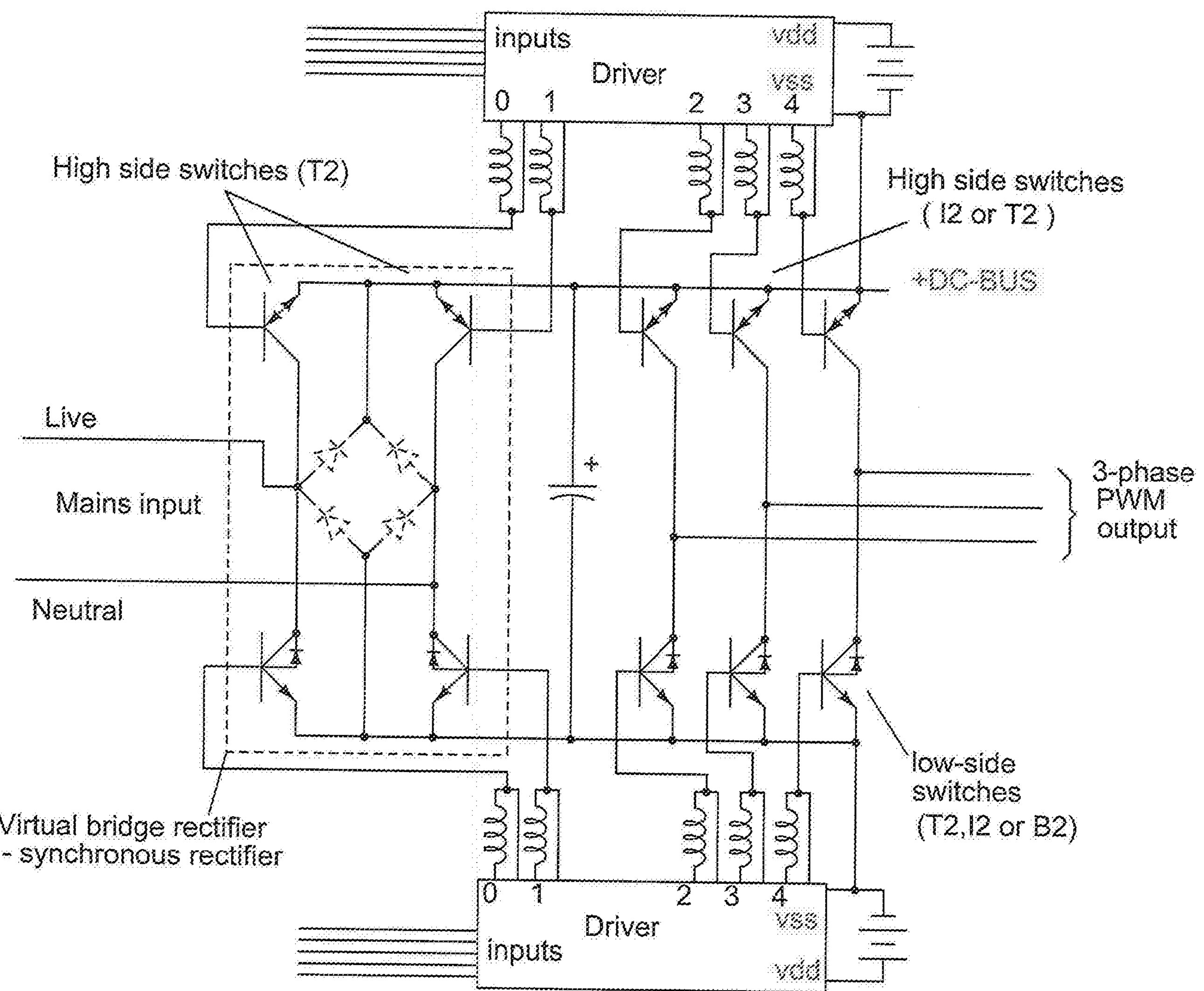


Fig. 36 - Efficient 3-phase inverter using DC bus, synchronous mains rectification



Note: Input level translators not shown. Aux. power supplies (Vdd/Vss) shown simplified